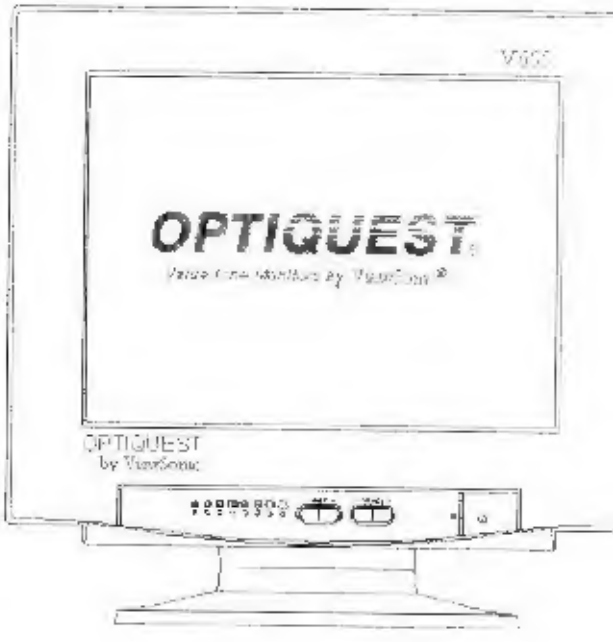
Service Manual

OPTIQUEST V65

Model No. V655-1M/1E/1

15" Digital Controlled Color Monito
Value Line Serie

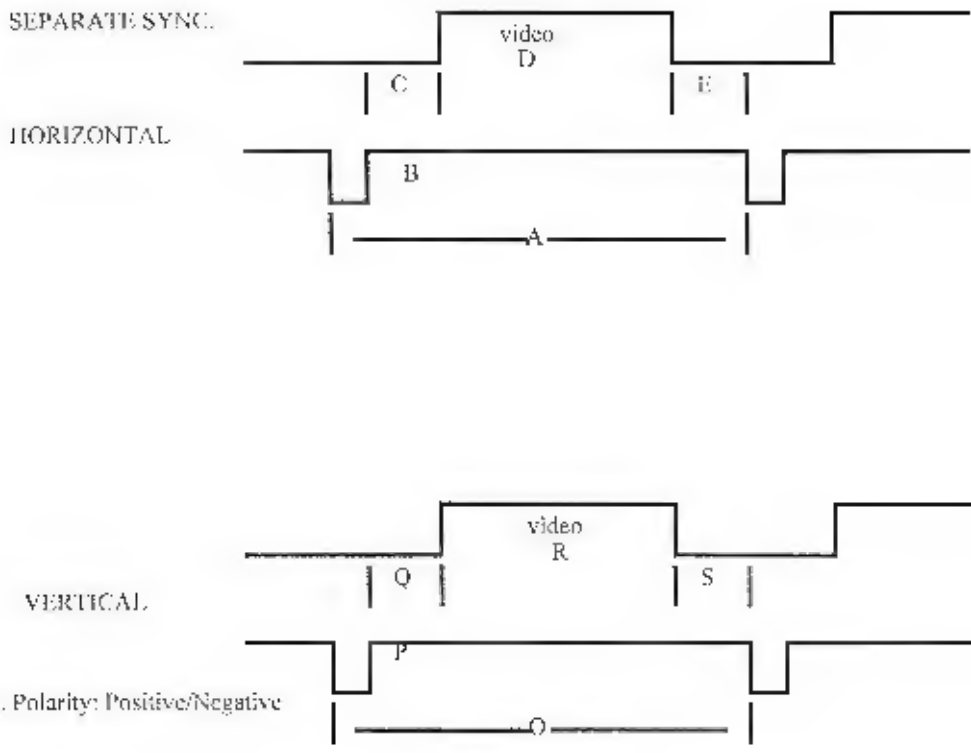


(Rev. 1 - July 199

ViewSonic® 20480 E. Business Parkway, Walnut, California 91789 USA - (800) 888-858

1.3.1.4 Timing

The video signal timing is as following:



PRESET TIMING

- VGA/SVGA Timing

	VGA400 Compatible	VGA480	VESA480	SVGA3	8514/A	UVGA1
(fH)	31.47KHz	31.47KHz	37.86KHz	48.09KHz	35.52KHz	48.36
(Aus)	31.77	31.77	26.413	20.794	28.15	20.67
(Bus)	3.81	3.81	1.270	2.399	3.92	2.229
(Cus)	1.59	1.59	4.603	1.279	1.25	2.622
(Dus)	26.05	26.5	20.317	15.995	22.8	16.78
(Eus)	0.318	0.318	0.762	1.119	0.18	0.393
(fv)	70.08	59.94Hz	72Hz	72.01Hz	87Hz	60.00
(Oms)	14.27	16.68	13.735	13.887	11.5	16.66
(Pms)	0.064	0.064	0.079	0.124	0.113	0.124
(Qms)	0.86	0.76	0.740	0.667	0.563	0.6
(Rms)	13.157	15.762	12.678	12.510	10.81	15.86

(Sms)	0.191	0.095	0.238	0.772	0.014	0.062

Display Resolution						
	640x400	640x480	640x480	800x600	1024x768	1024x
Polarity H/V Sync	-/+ separate	-/- separate	-/- separate	+/+ separate	+/+ separate	-/- separ

- 1024 X 768 Interlaced/Non-interlaced Timing

	UVGA2	WS2	VESA	Apple 16"	SuperMac 19'
Compatible					
(fH)	56.476KHz	64.317KHz	46.875KHz	49.71KHz	60.241KHz
(Aus)	17.707	15.55	21.333	20.115	16.6
(Bus)	1.813	0.97	1.616	1.118	1.2
(Cus)	1.920	2.24	3.232	3.911	2.2
(Dus)	13.653	11.96	16.162	14.528	12.8
(Eus)	0.320	0.37	0.323	0.559	0.4
(fv)	70.069Hz	60.393Hz	75Hz	74.533Hz	74.927
(Oms)	14.272	16.561	13.333	13.417	13.346
(Pms)	0.106	0.047	0.064	0.06	0.05
(Qms)	0.513	0.498	0.448	0.785	0.498
(Rms)	13.599	15.923	12.8	12.552	12.748
(Sms)	0.053	0.093	0.021	0.02	0.05

Display Resolution					
	1024x768	1280x1024	800x600	832x624	1024x768
Polarity H/V	-/-	+/+	+/+	-/-	-/-
Sync	separate	separate	separate	separate	separate

1.3.1.5 Input Signal Quality

(1) Rise/Fall time.
Video Signal : less than 3.5ns.
Horizontal SYNC : less than 50ns.
Vertical SYNC : less than 100ns.

(2) TTL Signal Level
The levels of Horizontal & Vertical SYNC will be TTL level; their high level will be 2.4-5.5V, and low level will be 0-0.2V.

(3) Video Signal Level
The video signal when terminated with an idea 75ohm termination will have a range of 0V to 0.7V (nominal), and its full scale output will be 0.7V and black level will be between 0V and 0.1V.

1.3.2 Power Supply Requirements

1.3.2.1 Power Management

The monitor handles the power saving modes according the final VESA specification with sync and V-sync recognition, The Amber power LED Blinks only at OFF mode as follows.

Mode	H-sync	V-sync	power	LED	Recovery Time
Normal	Active	Active	100W	Green	---
Stand-by	Inactive	Active	< 15W	Amber	3 sec
Suspend	Active	Inactive	< 15W	Amber	3 sec
off	Inactive	Inactive	< 5W	Amber Blinks	8 sec
Burn-In	Inactive	Inactive	> 30W	Green	---

*LED blinking duration 1.3 ⇧ 0.2 Sec.
The picture should appear within 10 seconds after the system is waked up.

The performance of unit should be in specifications within 30 minutes after the system waked up.

1.3.2.2 Input Power Requirements

(1) Input Voltage Range
The unit shall meet all the operating requirements with an input voltage range of 90 Vac.

(2) Input Current
Maximum

Input Current	Measuring Range
(MAX) 1.5 Arms	90Vac -- 264Vac

(3) Frequency Range
The unit shall operate within a frequency range of 47Hz to 63Hz.

(4) Inrush Current
Power supply inrush current shall be less than the ratings of its critical components (which includes power switch, fuse, rectifiers and surge limiting device) for all cond of line voltage.

(5) Regulator Efficiency
65% minimum (measuring at 115Vac and full load).

(6) Synchronization
The switching frequency of unit must be designed to synchronize with the horizonta frequency of the display unit.

(7) Power line Transient Immunity

The power supply shall function properly after being subjected to a 0.3us/1.2us, 200
high peak pulse, or 5ns/10ns, 1500 volt fast peak pulse applied either differentially o
endedly to line and neutral at any phase of the power line voltage and shall not caus
unsafe or unrecoverable errors.

(8) Maximum power consumption: 100 Watts. (without Audio signal input).

1.3.2.3 Output Power Requirements

The power circuit shall supply DC power outputs as follows:

Output	Nominal	Regulation	Load Current Range
1	50V	⇧3%	0.3-1A
2	75V	⇧3.5%	0.02A-0.15A
3	13.5V	⇧5%	0.6-1A
4	6.3V	⇧3.5%	0.51A-0.75A

1.3.2.4 AC Power Inlet

The display unit shall be supplied with an AC power NICOON NC-174, or equivalent, to be located at the rear of the display.

1.3.2.5 Power Cord

Each display unit shall be supplied with a power cord, with length of 1800mm king cord KC-003 or equivalent

1.3.3 CRT Requirements

The color picture tube used shall be a 15" 90 degrees, and shall have the following features:

-Type: 15" in-line, dot matrix.
-Dot pitch: 0.28mm dot triad.
-Phosphor: P22 or equivalent.
-Light transmittance: 57% (semi-tint).
-Surface of face plate: non-glare.

1.4 Functional Specifications

All the tests to verify specifications in this section must be performed under the following standard conditions unless otherwise noted. The standard conditions are:

-Temperature : 25 ⇧5 degree Celsius.
-Magnetic field : No additional magnetic field in near side, CRT faces to East.
-AC line input voltage : 90Vac to 264Vac. 50Hz or 60Hz.
-Warm-up time : 30 minutes minimum.
-Checking display mode : All the presetting modes, as 3.1.4 shown.

1.4.1 Display Quality

1.4.1.1 Display Data Area

(with 20 ft-l at full white pattern)

(1) Horizontal 270mm ⇧ 4mm
(2) Vertical 202mm ⇧ 4mm

1.4.1.2 Video AMP Performance

(1) Video bandwidth : 80MHZ
(2) Resolution : 1280 X 1024 (center)
(3) Output rise/fall time : 8.5ns

(4) Ringing : 10% max, first overshoot
4% max, second overshoot
1% max, third overshoot

(5) Sag : 5% max (at horizontal freq.)

1.4.1.3 Light Output

(1) At 3" block pattern (ABL is non-working) : 60Ft-L min.

(2) At full-white pattern (ABL is working) . 30 ⇧ 4FL Typical For VGA480

All the above is based on the conditions that brightness control, and contrast control are set at maximum position.

1.4.1.4 Contrast Adjustment Range : over 15Ft-L.

1.4.1.5 Brightness Adjustment Range

As contrast control is set at maximum level, adjusting Brightness control from minimum to maximum position, the light output of 3" block pattern shall be increased more than 20Ft-L. If adjusting Brightness control to minimum position, the 3" block pattern shall be extinguished when contrast control is set minimum also.

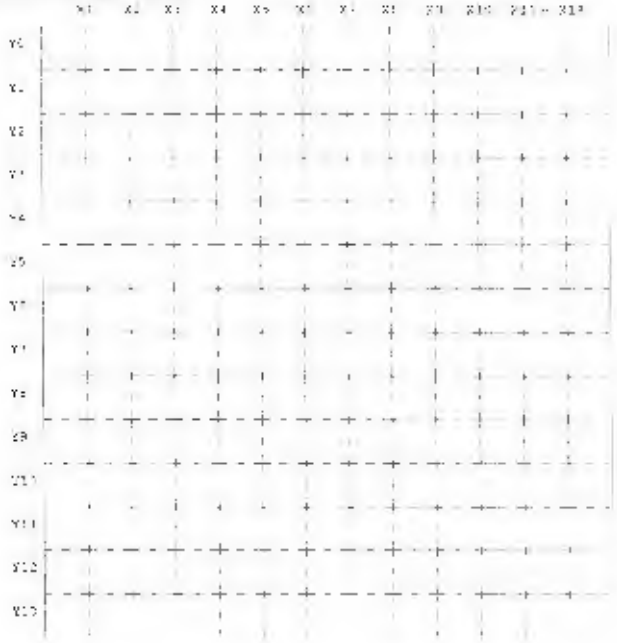
1.4.1.6 Linearity

(set to 20 Ft-L at full white pattern first) at crosshatch pattern:

(1) Vertical Non-linearity 5% max. as Fig.1

(2) Horizontal Non-linearity 5% max. as Fig.1

Fig.1 Linearity Measurements



$$\frac{Xmax - Xmin}{Xmax + Xmin} \times 100\%$$

$$\frac{Ymax - Ymin}{Ymax + Ymin} \times 100\%$$

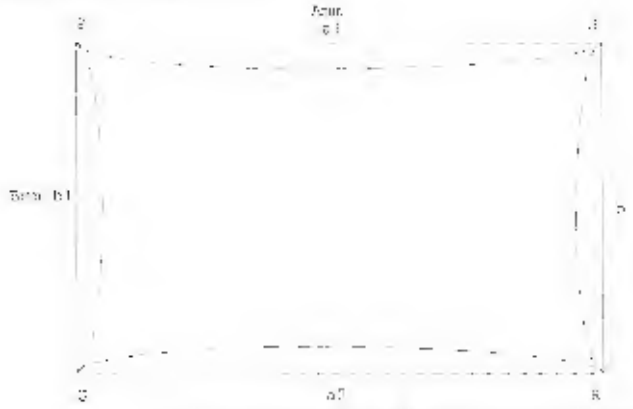
1.4.1.7 Geometric Distortion (with 20Ft-L at full white pattern)

Fig.2 Pincushion Measurements

(1) Top/Bottom Pincushion 1.5 mm max. as Fig.2 a1 or a2

(2) Side Pincushion 2.5 mm max. as Fig.2 b1 or b2

Fig.2 Pincushion Measurements

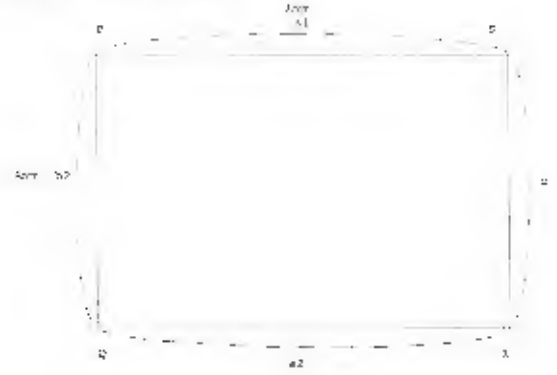


A, B represented as display area width and height
Top/Bottom Pincushion = (a1 or a2)
Side Pincushion = (b1 or b2)
substituted A by (PS + QR)/2
B by (PQ + RS)/2

(3) Top/Bottom Barreling 1.0 mm max. as Fig.3 a1 or a2

(4) Side Barreling 1.0 mm max. as Fig.3 b1 or b2

Fig.3 Barreling Measurements

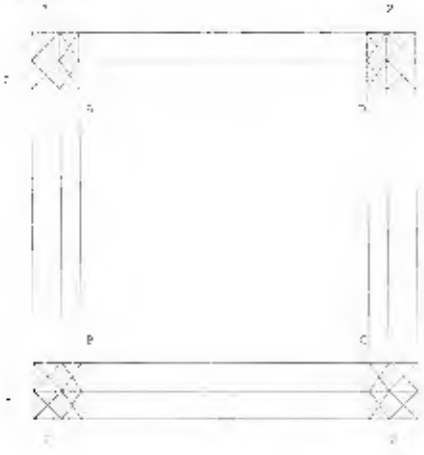


A, B represented as display area width and height
Top/Bottom Pincushion = (a1 or a2)
Side Pincushion = (b1 or b2)
substituted A by (PS + QR)/2
B by (PQ + RS)/2

(5) Vertical Trapezoid 2.0 mm max. as Fig

(6) Horizontal Trapezoid 2.0 mm max. as Fig

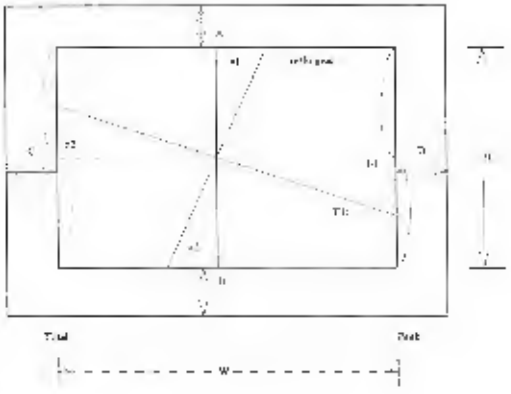
Fig.4 Trapezoid Measurements



* Each of the 4 corners of picture shall fall within the relevant area (F) illustra
above(hatched).
* ABCD is the picture outlines.

(7) Tilt 1.5 mm max. as Fig.5 b1 or b2
(8) Orthogonal 2.0 mm max. as Fig.5 a1 or a2
(9) Picture Centering 6.0 mm max. as Fig.5

Fig.5 Picture Distortion and Phase Measurements



V (Cent) = |A-B| < 4mm
H (Cent) = |C-D| < 4mm

1.4.1.8 Size Stability

Picture growth from 5 Ft-L to maximum Ft-L shall be less than 4mm with full white pattern (double side).

1.4.1.9 Swing & Jitters

Swing & Jitters are not permitted in the conditions stated as followings:(the distance of is 30cm from eyes to screen).

(1) AC power input fluctuated from 90Vac to 264Vac, 50Hz or 60Hz.

(2) Brightness & contrast VRs changed from max, to min. or vice versa.

1.4.1.10 Focus (The distance of viewing is 30cm from eyes to screen)

Under the condition of luminance of 20Ft-L at full-white pattern
(Brightness VR minimum, contrast VR adjusted), all # characters on the screen in the '
pattern will be clear.

1.4.1.11 DDC1/2B Table

Address	Data	Description
00	00	Header
01	FF	
02	FF	
03	FF	
04	FF	
05	FF	
06	FF	
07	00	
08	3E	ID Manufacturer Name =OQI
09	29	(VESA 3 character ID)
0A	32	ID Product Code =23
0B	33	(Vender Assigned code)
0C	*	ID Serial Number
0D	*	32 bits serial no.
0E	*	(use 0 if n/a)
0F	*	
10	*	Week of Manufacture (0-53),use 0 if n/a
11	*	Year of Manufacture (year - 1990)
12	01	EDID version
13	00	Revision
14	08	Video Input Define (see Note 1)
15	1B	Max. H. Image Size (cm)
16	14	Max. V. Image Size (cm)
17	A6	(gama*100) - 100
18	E8	DPMS (see Note 2)
19	0E	Red Green Bits Rx1Rx0Ry1Ry0Gx1Gx0Gy1Gy0
1A	6E	Blue White Bits Bx1Bx0By1By0Wx1Wx0Wy1Wy0
1B	A0	Red x bit9-2
1C	57	Red y bit9-2
1D	48	Green x bit9-2
1E	99	Green y bits9-2
1F	26	Blue x bit9-2
20	10	Blue y bit9-2
21	47	White x bit9-2
22	4F	White y bit9-2
23	A8	Established Timing I
24	FE	Established Timing II

25	00	Established Timing III (see Note 4)
26	01	Standard Timing Identification

Address	Data	Description
27	01	#1
28	01	#2
29	01	
2A	01	#3
2B	01	
2C	01	#4
2D	01	
2E	01	#5
2F	01	
30	01	#6
31	01	
32	01	#7
33	01	
34	01	#8
35	01	
36	00	Detailed Timing Description # 1
37	00	
38	00	
39	00	
3A	00	
3B	00	
3C	00	
3D	00	
3E	00	
3F	00	
40	00	
41	00	
42	00	
43	00	
44	00	
45	00	
46	00	
47	00	
48	00	Detailed Timing Description # 2
49	00	
4A	00	
4B	00	
4C	00	
4D	00	
4E	00	
4F	00	

Address	Data	Description
50	00	
51	00	
52	00	
53	00	
54	00	

Address	Data	Description
55	00	
56	00	
57	00	
58	00	
59	00	
5A	00	Detailed Timing Description # 3
5B	00	
5C	00	
5D	00	
5E	00	
5F	00	
60	00	
61	00	
62	00	
63	00	
64	00	
65	00	
66	00	
67	00	
68	00	
69	00	
6A	00	
6B	00	
6C	00	Detailed Timing Description #4
6D	00	
6E	00	
6F	00	
70	00	
71	00	
72	00	
73	00	
74	00	
75	00	
76	00	
77	00	
78	00	
79	00	
7A	00	
7B	00	

7C	00	
7D	00	
7E	00	Extension Flag
7F	*	Check Sum

Note 1

Bit	Bit Description
7	Analog / Digital Signal Level
6	Signal Level Standard (6)
5	Signal Level Standard (5)
4	Setup
3	Sync Inputs Supported (3)
2	Sync Inputs Supported (2)
1	Sync Inputs Supported (1)
0	Sync Inputs Supported (0)

Bit	Description
7	Analog / Digital Input : Defines usage of the rest of the byte as "analog input" or "digital input". Analog=0, Digital=1 . If input is described as ana the following definitions apply to bits 6-0. Digital is as yet undefined in following but provisions have been made in anticipation of a common v output standard for Flat Panel Display (FPD) use.
6:5	Signal Level Standard (6:5) : Refer to the following bit definitions. Identif by the level of reference white volts above blank, followed by the level o sync tips in volts below blank. Bit 6 / Bit 5 / Operation 0 / 0 / 0.700V/0.300V (1.000V p-p) 0 / 1 / 0.714V/0.286V (1.000V p-p) 1 / 0 / 1.000V/0.400V (1.400V p-p) 1 / 1 / Reserved; TBD
4	Setup: If set, the display is set to expect a blank-to-black setup or pede per the appropriate signal level standard.
3:0	Sync Inputs (See Bit Operation below)
	3 — Separate Sync
	2 — Composite Sync (on H Sync line)
	1 — Sync on Green Video
	0 — Serration of the V.Sync Pulse is required when composite sync sync-on- green video is used

Note 2

Bit 7	Stand-by
Bit 6	Suspend
Bit 5	Active off
Bit 4:3	Display Type
	0,0 - Monochrome/gray scale display 0,1 - RGB color display 1,0 - Non-RGB multicolor display (example:RGY) 1,1 - Undefined.
Bit 2:0	Reserved. Set at 00h until defined.

Note 3

CRT Vender	Red (x/y)	Green (x/y)	Blue (x/y)	Gamma
Hitachi	0.625/0.340	0.285/0.600	0.150/0.065	2.66

Note 4

Byte 1	bit	Established Timings 1	Source
	7	720x400 @ 70Hz (640x400)	(VGA, IBM)
	6	720x400 @ 88Hz	(XGA2, IBM)
	5	640x480 @ 60Hz	(VGA, IBM)
	4	640x480 @ 67Hz	(Mac II, Apple)
	3	640x480 @ 72Hz	(VESA)
	2	640x480 @ 75Hz	(VESA)
	1	800x600 @ 56Hz	(VESA)
	0	800x600 @ 60Hz	(VESA)
Byte 2	bit	Established Timings II	
	7	800x600 @ 72Hz	(VESA)
	6	800x600 @ 75Hz	(VESA)
	5	832x624 @ 75Hz	(Mac II, Apple)
	4	1024x768 @ 87Hz (interlaced)	(IBM)
	3	1024x768 @ 60Hz	(VESA)
	2	1024x768 @ 70Hz	(VESA)
	1	1024x768 @75HZ	(VESA)
	0	1280x1024@75HZ	(VESA)
Byte 3	bit	Manufacturer's Timings	Manufacturer's Specified Timing
	7	1152x870, 75Hz	(Mac II, Apple)
	6	Reserved	Manufacturer's Specified Timing

	5	Reserved	
	4	Reserved	
	3	Reserved	
	2	Reserved	
	1	Reserved	
	0	Reserved	

1.4.2 Color Quality

1.4.2.1 Misconvergence

Use "crosshatch" white pattern, then set the brightness VR until the raster disappear and set & contrast VR to its max to examine the convergence. The misconvergence must strictly meet the requirements stated as follows:

1.4.2.2 Moiré (the distance of watch is 30cm from eyes to screen)

In the pattern of all green, all blue, all red, or all white, and the luminance is higher than moiré is not allowed to appear.

1.4.2.3 Impurity

Impurity should not appear in the pattern of all green, all blue, all red, or all white. The brightness is 0~max Ft-L and the screen display is set to east direction.

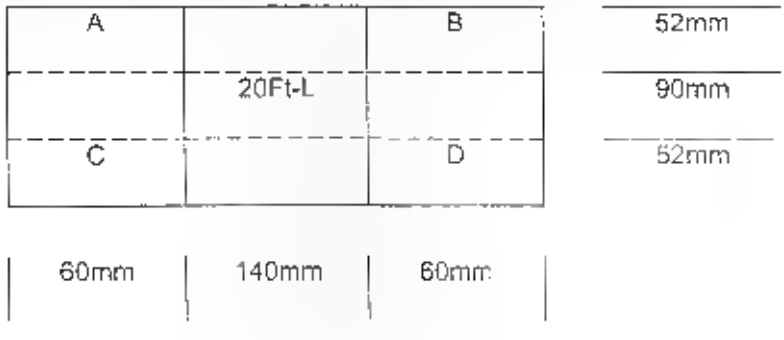
1.4.2.4 White Balance

At the condition of all white pattern, X=0.281, Y=0.311, white balance is required to meet the following specifications when brightness VR set until the raster disappear and contrast VR changed at 3" block pattern.

40 Ft-L = X, Y variety value < 10%
20 Ft-L = X, Y variety value < 10%
5 Ft-L = X, Y variety value < 20%

1.4.2.5 Uniformity

When the display unit is displayed with mosaic pattern at the central brightness of 20 F corners (A,B,C,D) brightness must be >= 14 Ft-L.



Indicator of Testing Positions

1.4.2.6 Degaussing

Degaussing shall occur automatically when the monitor is turned on and shall be sufficient to demagnetize the CRT to any possible change in Earth's magnetic field, caused by moving or shipping operation. It should be cooled down at least 20 minutes power off before power on.

1.4.3 Controls & Presetting

User Control (on the front panel)

(1) Power on/off switch--rocker switch.

(2) Select Tact Buttons Switch.

(3) Adjust Tact Buttons Switch.

* Item (2), (3) are digital controls

1.5. Physical Specifications

1.5.1 Physical Dimension ■ Appearance

Overall Dimensions: 376mm (W) X 373mm (H) X 385mm (D).

Net Weight: 12.5kgs.

Outer Appearance: see Fig.6 & Fig.7

Fig.6 Physical Dimension: Front View

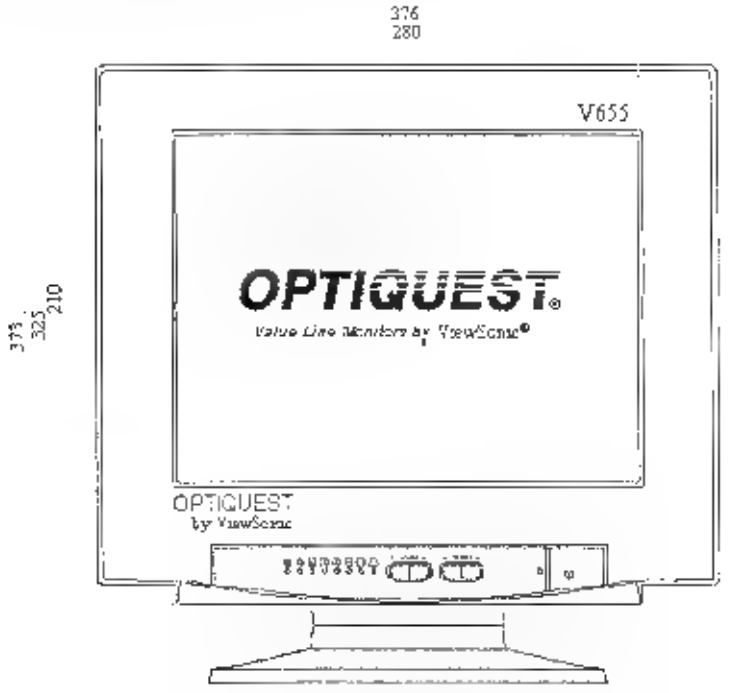
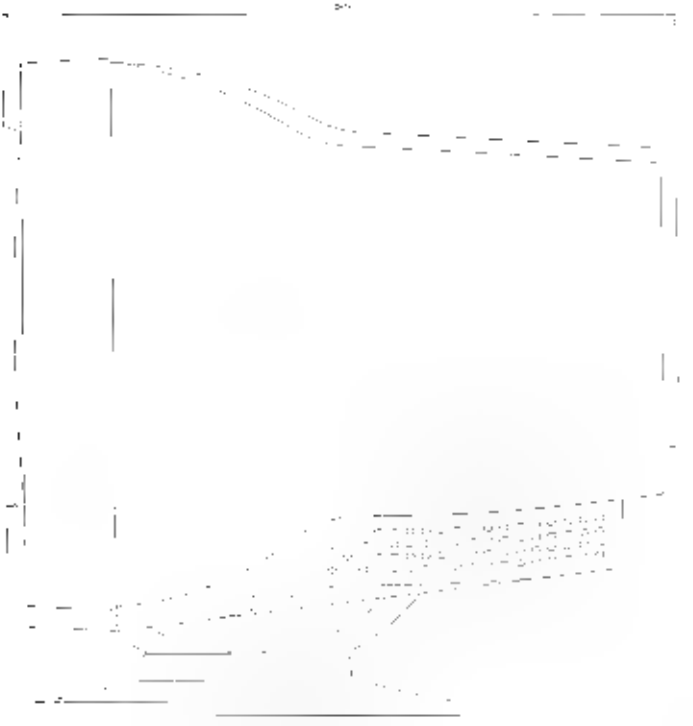


Fig.7 Physical Dimension: Side View



1.5.2 Construction and Materials on Outer Surface

-Materials: Plastic
-Color: Light Gray

1.5.3 Base & Swivel

-Tilt: -5/+15 degrees
-Swivel: -45/+45 degrees

1.5.4 Marking & Labels

1.5.4.1 Reference Label (Rear panel)

(1) Reference numbers
(2) Manufacture data
(3) Agency approvals
(4) Power ratings

1.5.4.2 Controls & Connectors

(1) AC power cord input: abbreviated labels
(2) User's controls: standard print

1.5.5 Packaging

Carton Dimension: 492mm (L) x 460mm (W) x 460mm (H)

Shipping Weight: 14.5kgs.

CIRCUIT OPERATION THEORY

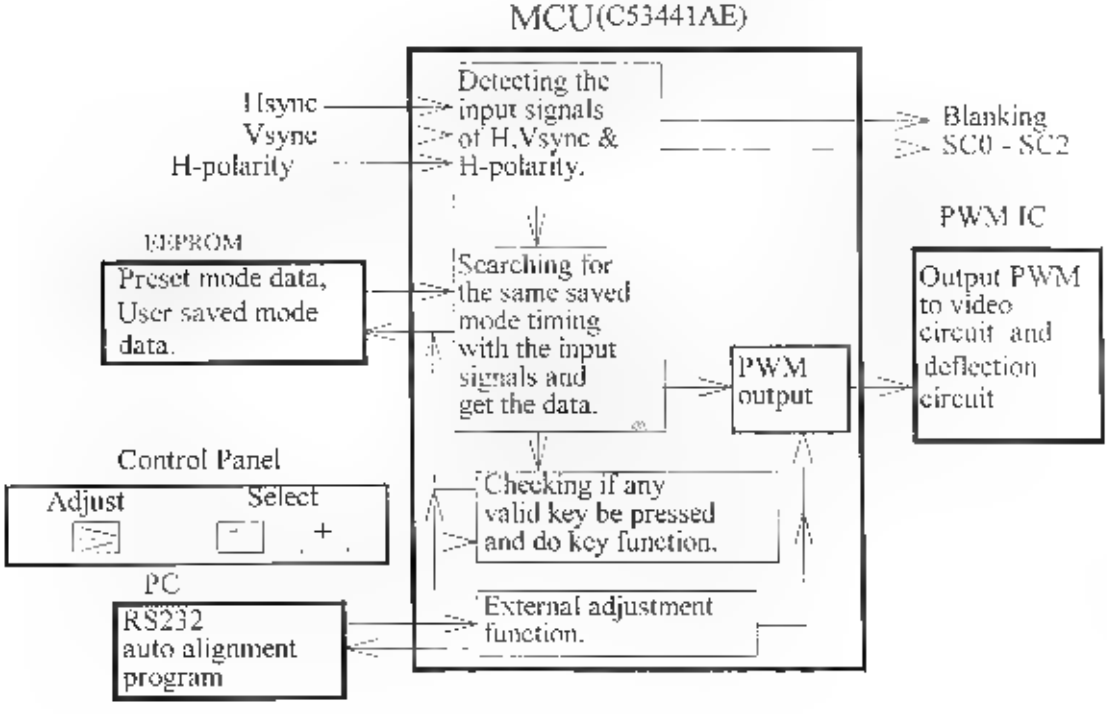
2.1 Foreword

The purpose of using micro-controller, which has both hardware and software function, in the display unit, is to reduce the volume of circuits used in the display; and, using the advantage of input frequency detection and digital output control, to store data of various modes of digital display frequency. It's indispensable for a factory doing efficient automatic adjustment operations and outputting uniform quality units.

2.2 Digital Circuit Operation Theory

2.2.1 Block Diagram

The major parts of the V655 microcontroller circuit are MCU, EEPROM, and PWM IC. The block diagram is shown below:

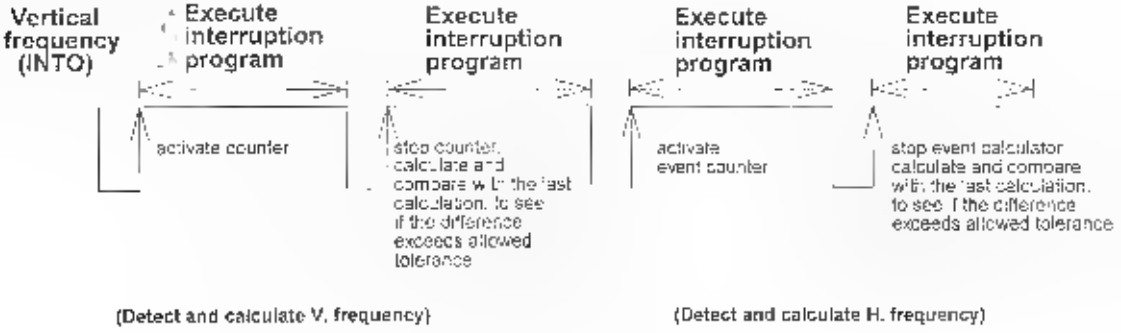


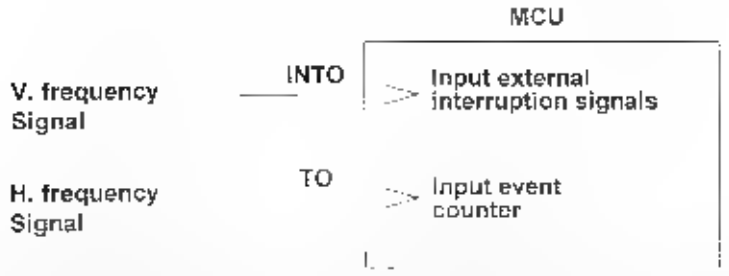
2.2.2 Function Description of Components

(a) MCU

The MCU is C53441AE. It is an 87C51 with PWM output controlled microcontroller. It manages the following functions:

(1) To detect the mode and output the correct SC0, SC1 and SC2 to deflection circuit.



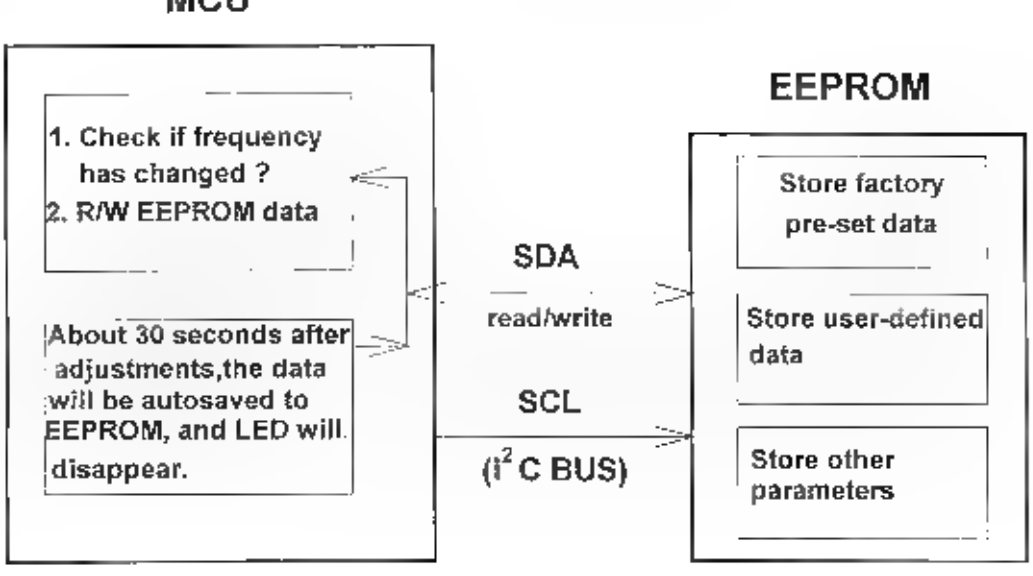


(2) To check if there is the same saved mode in the EEPROM and get the data to transfer into DC voltages by PWM output and RC filter circuits to control the picture, color, contrast and brightness.
(3) To check if the valid key is pressed and to do the key function.
(4) To memorize mode timings and any adjustable parameters of the picture onto EEPROM.
(5) Through UART(Universal Asynchronous receiver Transmitter), the internal register value of Micro-controller and output value of PWM can be communicated through serial port with external PC. The automatic adjusting operations in the factory are done through this function.

(b) EEPROM

The EEPROM of the V655 is a 24C04 which adopts I^2C bus to do the data transfer job. It uses two data lines to communicate, through serial data transfer, with MCU for data reading and writing operation.

The MCU will store the digital displaying data of the display unit into a pre-assigned block in the EEPROM. It will access these data under certain conditions. The block diagram is shown below:

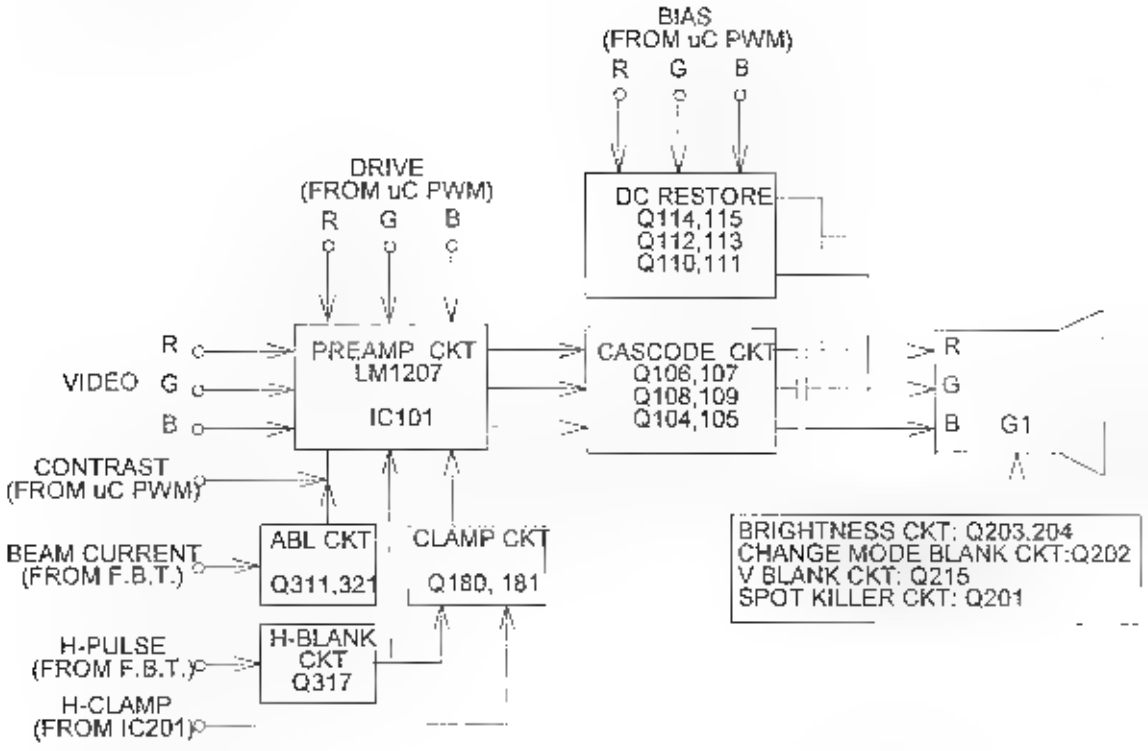


(c) PWM IC:

PWM IC, its code no. is AP3105 IC, transfers data through serial bus. The format of PWM IC is as follows:

Bit 17 : 1= enable / 0--disable
Bit 16 : 0
Bit 15 - 8 : Address
Bit 7 - 0 : data

2.3. VIDEO CKT



2.3.1 OSD Preamp CKT

(a) As shown in the block diagram:
the R/G/B signals, amplified by two amplifiers, will generate enough amplitude of Vpp to show up on the CRT screen. The first one, the preamp CKT, processes the signal and mixes up the OSD. The second one does the power amplification.

(b) OSD preamp IC101, LM1281 will output the R/G/B signals separately. The R/G/B driver will control the gain of these three guns individually to approach the white balance of the CRT. Then the CONTRAST (from UC AP3104) controls the gain of these three guns simultaneously.

(c) The purpose of the signal clamp is to fix the black level of all R/G/B signals to the same level after the AC coupling. This is the DC restoration of the pre-amplifier.

(d) The signal H-Blank is to let the output of LM1207 be pulled down to 0.2V, during non-display mode. Then the cascade CKT will generate a level higher than black level (i.e. Sync Tip), therefore the video will be blanked in order to prevent the fold over occurring when adjusting H-phase. Besides, the Sync Tip is used for the DC Restoration of cascade CKT.

(e) LM1281 is equipped with an OSD mixer. When signal CUT is low, the output of LM1280 is video signal. When signal CUT goes high, the output will be OSD signal.

2.3.2 Cascade CKT

Output stage uses cascade circuit. Its purpose is to amplify the signal which has been processed by LM1207 to enough amplitude of Vpp, then it is displayed on the CRT. The criteria to select a cascade transistor is: the smaller the value of Cob and the larger the value of Ft the better. This circuit adopts BFQ235A. Cob=2pF, ft=1GHz.

2.3.3 DC Restore CKT

(a) The video signal amplified by the output stage is coupled to CRT by way of AC coupling. So the DC restoration CKT is needed to do the white balance adjustment.
(b) This DC restoration circuit adopts SYNC TIP CLAMP. While Sync Tip lasts the capacitor charges. At other times it discharges. The black level is kept to the level of DC restoration set by UC.

2.3.4 ABL CKT (Auto Brightness Limit)

ABL is a protection circuit. When the anode current goes higher than the setting value of the ABL circuit ABL will pull down the voltage of contrast to limit the anode current. This is helpful to protect the CRT.

2.3.5 H-Blank CKT

After the collect pulse which comes from FBT is shaped and inverted, it will be sent to preamp CKT and used as the H-blank.

2.3.6 Clamp CKT

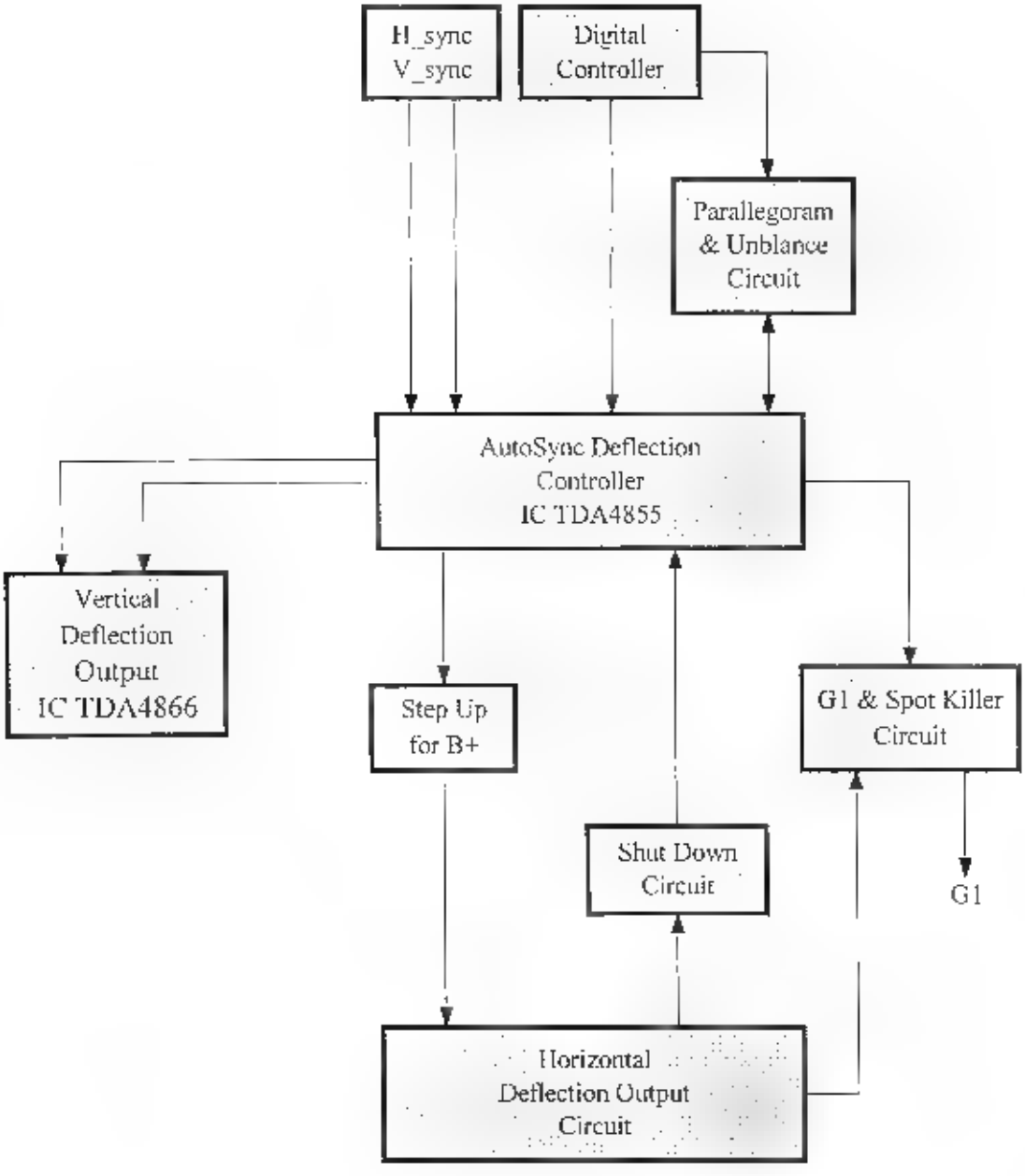
The two sources of clamp pulse are:
The first comes from IC201 when in normal status. The second, since there is no output of H-clamp pulse from IC201 during Free Run, will be shaped and inverted before sent to preamp.

2.3.7 Brightness, V-Blank, Change Mode Blank, Spot-killer CKT

(a) When the voltage of cathode to G1 goes over the cut off voltage , the picture will disappear. If the cut off voltage of the CRT G Gun is set at 110V and the black level of the cathode is 60V, the picture won't show the signals higher than the black level once the G1 voltage is lower than -50V.
(b) As described above, we may use the voltage to control G1 as the brightness control. Generally the G1 control range is about 10-15V, if the Raster brightness is from 0 to 1.5ft-L.
(c) Similarly, we may overlap a negative pulse of vertical duration on the G1 voltage to prevent the vertical retrace line from showing on the picture. This is to keep the voltage cathode to G1 over the cutoff voltage, during the period of vertical retrace.
(d) In order to avoid the picture occurring transiently while in change mode, pull down the G1 voltage and let the voltage cathode to G1 go over the cutoff voltage. This will cause the picture to blank.
(e) While the monitor is turned off, the discharge speed of the high voltage circuit is slow Since there is no deflection scan acting on the electronic beam, a spot, which will destroy the phosphor of the CRT, will display on the CKT. So the spot-killer circuit will generate a negative voltage higher than cutoff to the G1 to cut the beam. This will protect the CRT.

2.4. DEFLECTION CKT

2.4.1 Block Diagram for the V655 Deflection CKT



2.4.2 Horizontal and Vertical Oscillation Circuit

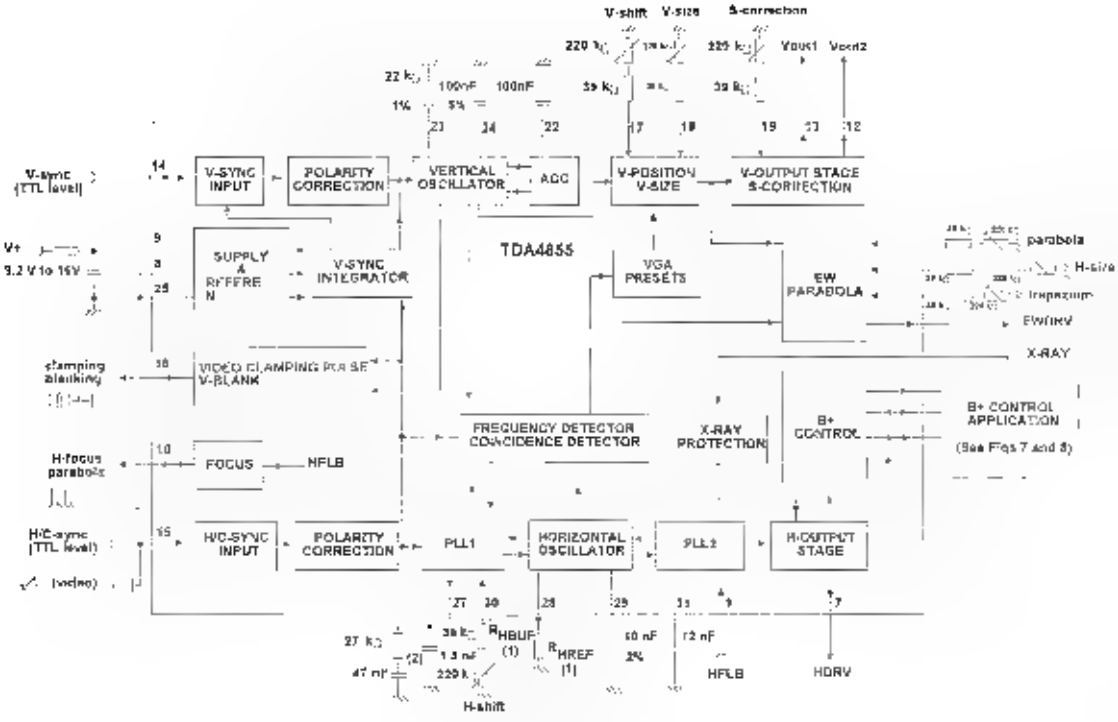
IC201 TDA4855 merges the horizontal oscillation stage and vertical oscillation stage.

2.4.2.1 The Pin Assignment of IC201 TDA4855:

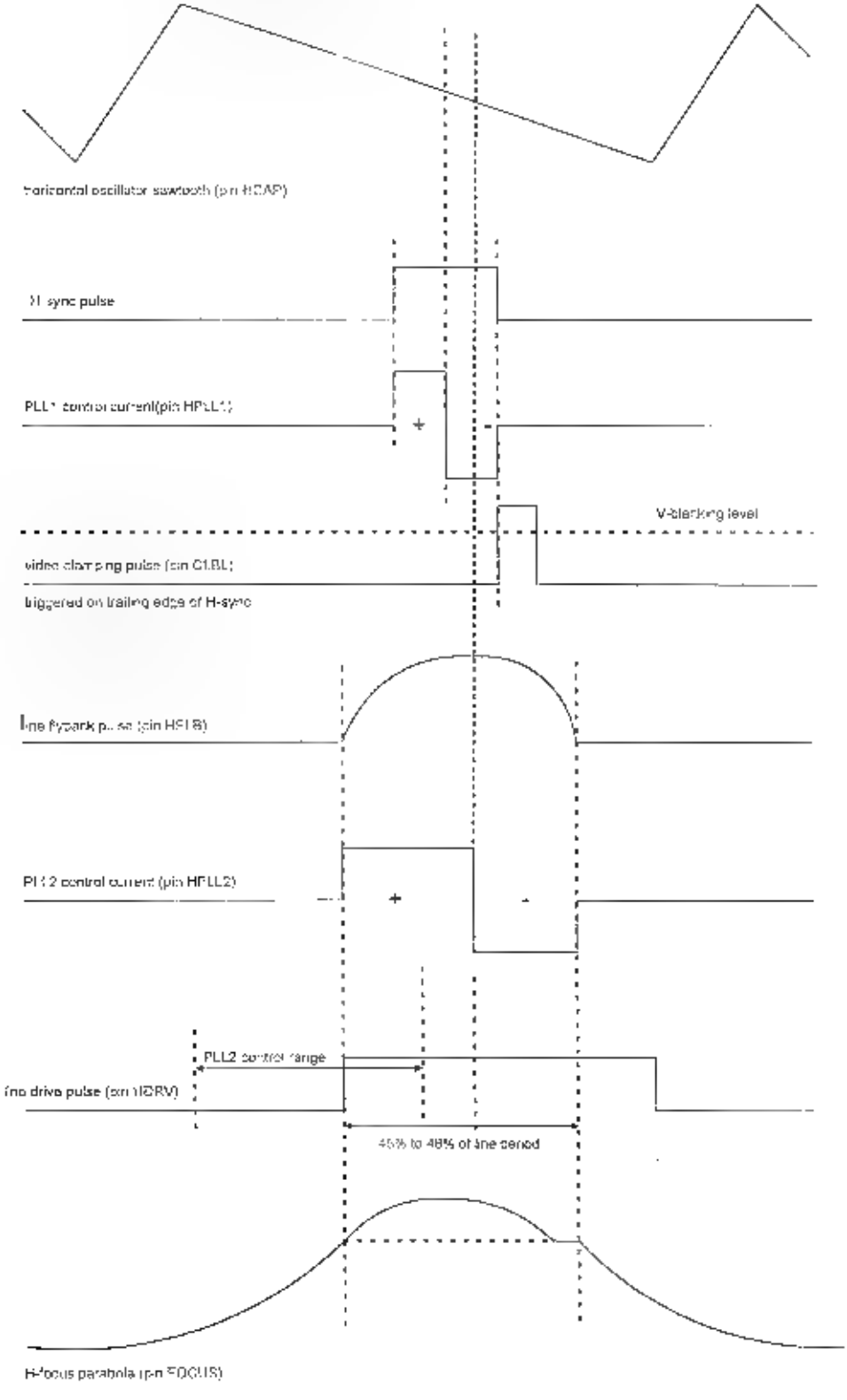
TDA4855 PINNING

SYMBOL	PIN	DESCRIPTION
HFLB	1	horizontal flyback input
XRAY	2	X-ray protection input
BOP	3	B+ control OTA output
BSENS	4	B+ control comparator input
BIN	5	B+ control OTA input
BDRV	6	B+ control driver output
HDRV	7	horizontal driver output
GNDP	8	ground (power ground)
Vcc	9	positive supply voltage
FOCUS	10	H-focus parabola output
EWDRV	11	EW parabola output
VOUT2	12	vertical output 2 (ascending sawtooth)
VOUT1	13	vertical output 1(descending sawtooth)
VSYNC	14	vertical sync input / output
HSYNC	15	horizontal / composite sync input
CLBL	16	video clamping pulse / V-blanking output
VPOS	17	V-shift input
VAMP	18	V-size input
VSCOR	19	vertical S-correction input
EWTRP	20	EW trapezium correction input
EWPAR	21	EW parabola amplitude
VAGC	22	external capacitor for V-amplitude control
VREF	23	external resistor for vertical oscillator
VCAP	24	external capacitor for vertical oscillator
GNDS	25	ground (signal ground)
HPLL1	26	external filter for PLL1
HBUF	27	buffered f/v voltage output
HREF	28	reference current for horizontal oscillator
HCAP	29	external capacitor for horizontal oscillator
HPOS	30	H-shift input
HPLL2	31	external filter for PLL2 / soft start
EWWID	32	H-size input

2.4.2.2 TDA4855 Block Diagram



2.4.2.3 Horizontal Timing Diagram for TDA4855



2.4.2.4 Autosync Oscillator Control

The frequency-locked loop can lock the H-oscillator over a wide frequency range. This is achieved by a combined search and PLL operation. The frequency range is preset by two external resistors and can reach a maximum ratio of f_{MIN}/f_{MAX}=1/3.5. Larger ranges are possible by extended applications.

Without a H-sync signal, the oscillator will be free-running at f_{MIN}. Any change of sync conditions is detected by the internal coincidence detector. A deviation of more than 4% between H-sync and oscillator frequency switches the horizontal section into search mode. This means that PLL1 control currents are switched off immediately. Then the internal frequency detector starts tuning the oscillator. Very small DC currents at pin PLL1 are used to perform this tuning with a well defined change rate. When coincidence between H-sync and oscillator frequency is detected, the secrete mode is replaced softly by a normal PLL operation. This operation ensures a smooth tuning and avoids fast changes of H-frequency during catching.

In this concept, it is not allowed to load pin HPLL1. The frequency dependent voltage at pin HPLL1 is fed internally to pin HBUF via a sample and hold and buffer stage. The sample and hold stage removes all disturbances caused by H-sync or composite V-sync from the buffered voltage. An external resistor from HBUF to HREF defines the frequency range.

$f_{MAX}=f_{S(MAX)}*1.06$ $f_{MIN}=f_{S(MIN)}/1.087$

$$R_{HREF}=\frac{74KHz.K\Omega}{f_{MAX}}$$

$$R_{HBUF}=R_{HREF}.\frac{1.18.n}{n-1}$$

$$n=\frac{f_{MAX}}{f_{MIN}}$$

2.5. VERTICAL OUTPUT CIRCUIT

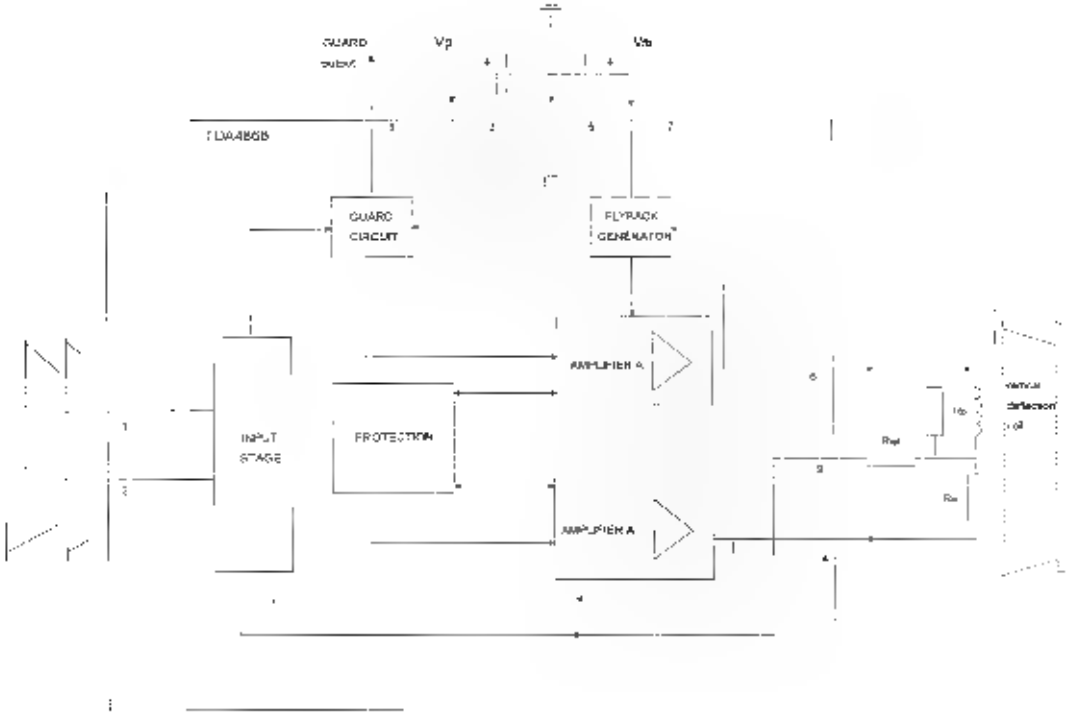
2.5.1 TDA4866

IC202 TDA4866 is used for vertical output amplifier.

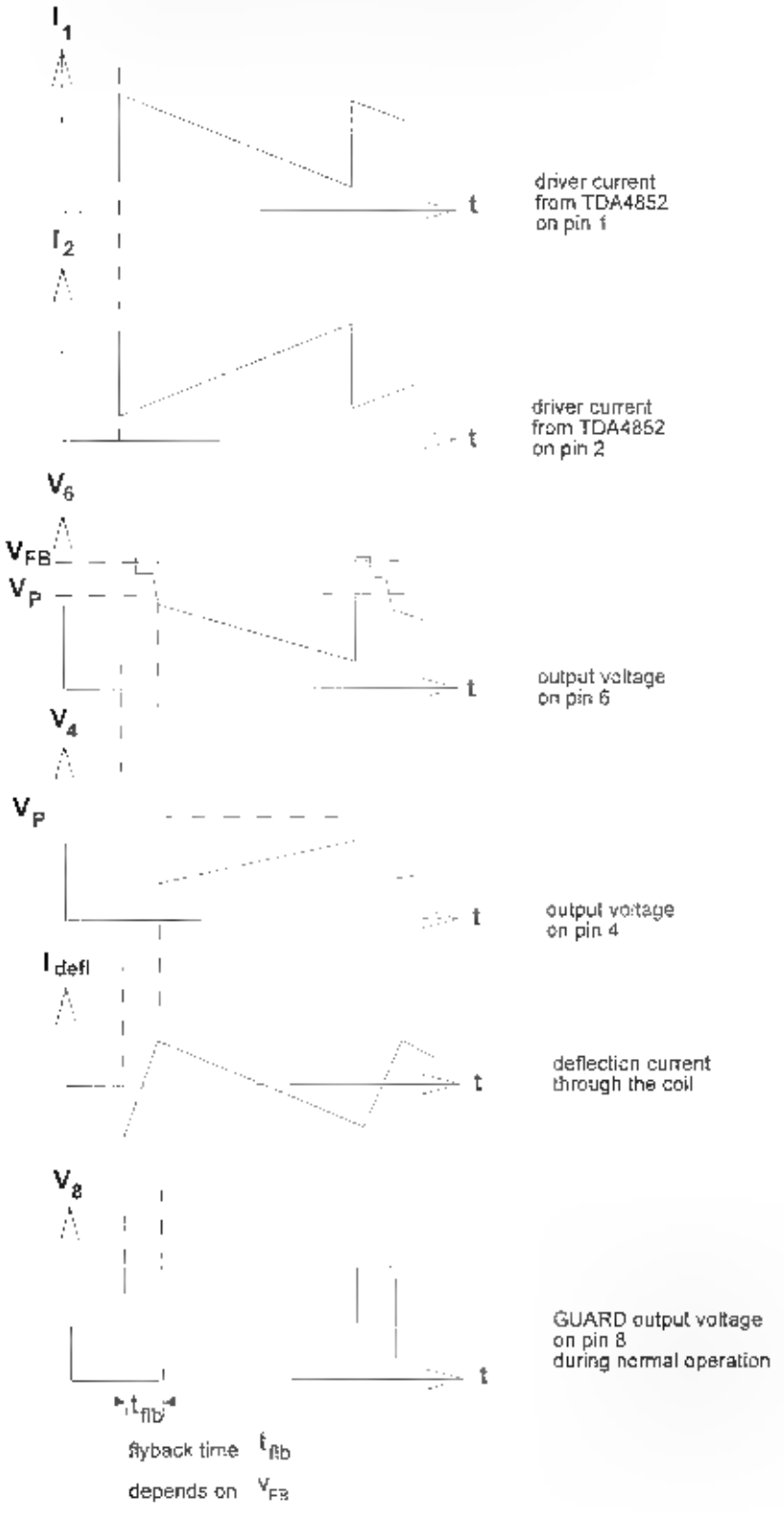
The pin assignment of IC202 TDA4866:
Pin 1 : Vertical oscillation input 1.
Pin 2 : Vertical oscillation input 2.
Pin 3 : Vcc, +12VDC.
Pin 4 : Vertical output V-.
Pin 5 : Ground.
Pin 6 : Vertical output V+
Pin 7 : Flyback supply voltage +40VDC.
Pin 8 : Vertical blanking pulse.
Pin 9 : Feedback input.

Q215 send the vertical blanking pulse to GT.

Block Diagram:



IC TDA4866 Timing Diagram, for the V655 vertical:



2.5.2 Autosync

Normalized composite-sync signals from pin HSYNC are integrated on an internal capacitor in order to extract vertical sync pulses. The integration time is dependent on the II-oscillator reference current at pin HREF. The integrator output directly triggers the vertical oscillator. Furthermore this signal is available at pin VSYNC (normally V-sync input), which is used as an output pin in this mode.

V-sync signals (TTL) applied to pin VSYNC are sliced at 1.4V. The output signal of the sync slicer is integrated on an internal capacitor to detect and normalize the sync polarity.

If a composite-sync signal is detected at pin HSYNC, pin VSYNC is used as output for the integrated V-sync (e.g. for power-saving applications).

V-Center Adj:
Pin 13 & pin 12 of IC201 send sawtooth signals to Pin 1 & Pin 2, to control V-shift.

2.6 H-Driver & Output CKT

Pin 7 of IC201 is H-driver, and drives transformer T302 by Q301.

Q302 is H-output transistor. Q302, D303 and D304 are combined into Diode Modulation CKT. It can stabilize HV, make large sidepin control range and control H-size. D302 is Speed-up CKT. It reduces t_f of Q302 and power loss. R304 is Current-restriction resistor. Q302 provides the scanning of right-side screen, and D304 for the left side.

Cs compensator CKT:
C309 is used for Cs correction. There are different correcting values for different frequencies, so we add C310, C311 and C330. In order to compensate Cs, uc sends signals SC_0~SC_2 to control C310, C311 and C330.

	SC2	SC1	SC0
FH < 31K	0	0	0
31K ≤ FH < 36K	0	1	0
36K ≤ FH < 45K	0	0	1
45K < FH < 58K	0	1	1
58K ≤ FH < 70K	1	1	1

2.7 Step-Down CKT, HV. Adj. and H-Center CKT

B+ for FBT is supplied by Step-Down CKT. Q316 is switched ON & OFF by BDRV(Pin 6 of TDA4855) and the energy of L304 is released to form Step-Down. The CKT is supplied by a fixed 185V to get various B+ depending on various BDRV.

VR203 is used for high voltage adjustment. It controls the DC level of BOP (pin 3 of TDA4855) and the size of sawtooth signal of BSENS (pin 4 of TDA4855). When the interval of BDRV changes, so does B+.

HPOS, pin 30 of TDA4855, provides a linear adjustment of the relative phase between H-sync and HDRV.

2.8 HV Shut Down CKT

When HV increases, the DC level of FBT pin 3 increases too. And XRAY, pin 2 of TDA4855, a voltage detector, forces TDA4855 to shut down.

2.9 G1 & Spot Killer CKT

While power is on, C211 remains 75-(-91-91)=257V. At the point of power-off, -75V becomes 0V and the negative side of C211 becomes -257V. Then the emitter of Q201 becomes -252V, while the base of Q201 equals -182V. And when Q201 is ON, and G1 equals -252V, the screen will be turned off.

If Blanking is active and Q202 is ON, then Q203 will be OFF and G1 will be -182V.

Alignment Procedure

3.1 Preliminary Adjustment

A. Pre-set all VRs to the center position
B. Set up unit and keep it warm up at least 30 minutes
C. Signal mode:

(Table 1)

Mode	Resolution	Fh	Fv	H/V
VGA	640x400	31.47KHz	70Hz	-/+
VGA	640x480	31.47KHz	60Hz	-/-
VGA	640x480	37.86KHz	72Hz	-/-
SVGA	800x600	48.09KHz	72Hz	-/-
8514	1024x768	35.52KHz	87Hz	-/+
UVGA	1024x768	48.37KHz	60Hz	-/-
UVGA	1024x768	56.48KHz	70Hz	-/-
WS	1280x1024	64.32KHz	60Hz	+/+
VESA	800x600	46.87KHz	75Hz	+/+
MAC	832x624	49.71KHz	75Hz	-/-
MAC	1024x768	60.24KHz	75Hz	-/-

3.2 B+ Adjustment

a. Input mode 48KHz (SVGA III 800x600) with cross hatch pattern
b. Set brightness and contrast keys to maximum position
c. Adjust VR 601, set the o/p of 13.5 ± 0.1V

3.3 High-Voltage Adjustment (48KHz Crosshatch SVGA III)

a. Adjust VR 203 set H.V to 25 ± 0.2KV

3.4 Geometry Adjustment

a. Input full white pattern of 64.317KHz (WS2 1280x1024) mode.
b. Adjust H-center (VR 302) to let the raster be in the center of both edges.
c. Input full white pattern of 49.71KHz (Apple 16" 832 x 624) mode.
d. Adjust H-width to max. Then readjust internal VR202 to let H-size equal to full size.
e. Input full white pattern of 48KHz (SVGA III 800x600) mode.
f. Power off, press sel+ & adj- Power on and adjust HxV size equaling to 270x202 mm.
g. Adjust HxV be equal to 270x202 mm for all factory setting mode (see Table 1).

key define

option

	sel-	sel+	adj-	adj+	
bit	1	2	3	4	(bit 0 reserve)

factory mode	---->	sel+ & adj-	(power on)
final check mode	- - ->	sel+ & adj+	(power on)
save	- - >	sel- & adj-	(factory only)
clear factory	---->	sel- & adj+	(factory only & 3 times)
clear user area	====>	adj- & adj+	(factory only)
recall	====>	sel+ & adj-	(user only)
tilt adjust key	====>	sel+ & adj+	(user only)

LED define

LED

1	2	3	4	5	6	7	8

	user area LED ON	factory LED OFF
1	brightness	B drive
2	contrast	B bias
3	H size	G bias
4	H phase	G drive
5	V size	R bias
6	V center	R drive
7	pin	unbalance
8	Trapezoid	parallel
7&8	tilt	tilt

3.5 Color Temperature Auto Alignment

A. PREPARING ITEMS

a. PC
b. RS232 BOX
c. RS232 CABLE (9P) TO PC
d. RS232 BOX TO MONITOR CABLE (3P)
e. COLOR ANALYZER (CA100)
f. CA100 CABLE TO PC
g. ADJUST PROGRAM (refer to attached floppy version 1.1)

B. Alignment Procedure

a. Adjust the G2 VR such that
the max. color of R.G.B color bar on the monitor is in the mark region
b. Auto color temperature adjustment
9300K X= 281 ± 5 Y= 311 ± 5
c. Adjust VR301 ABL adjustment to let
Y= 30Ft-L ± 1 Ft-L

3.6 Focus Adjustment

a. Input SVGAIII with # pattern
b. Adjust the focus VRs of T301 FBT until picture is clearest

3.7 Convergence Adjustment

a. Input video VGA480 with crosshatch pattern.
b. Then degauss CRT face.
c. Adjust 4-pole and 6-pole of DY, check that the convergence meets the spec.
d. If there is impurity between CRT and yoke, add convergence magnet by using magnets.

3.8 Energy Saving Function

a. Compliant with VESA proposal
b. With Normal/Stand-by/Suspend modes
c. keep on more than 1 ± 0.2 seconds to judge stepping into suspend mode

Table 6 :
display power management.

Mode	H-Sync	V-Sync	LED Power Consumption		Recover Time
Normal	on	on	Green	100W	0 sec
Stand-by	off	on	Amber	≤ 15W	3 sec
Suspend	on	off	Amber	≤ 15W	3 sec
Off	off	off	Amber Blinks	< 5W	8 sec

d. Input CHROMA-1000 VGA1 with color BAR pattern
e. Normal mode check:
Turn on the power switch (1); If the LED power indicator is "Green", then check if "D
Power Meter" is 100 watts.
f. Stand-by & suspend mode check:
Use EXT-control software to make H-Sync-Off & V-Sync-On, or V-Sync-Off & H-Sync
If the power LED indicator is "Amber", then check if the "Digital Power Meter" is ± 15 watts.
g. Off mode check:
Quit the EXT-signal (signal cable connected to CHROMA 1000), then check if "D
Power Meter" is ± 5 watts.
h. Free-run mode check:
Disconnect signal cable. Turn off the power switch (0). Then turn on the power switch (1) and check if the Raster Light output is free running.

3.9 DDC Writer Alignment Procedure

(1) Overview

The DDC writer tool include : 8255 control card
Barcode reader (option)
Files : (1) PD133.EXE
(2) PDO33.EXE
(3) QA33.EXE
(4) DDC.WEK
(5) ***.DDC

(2) File introduction

(a) File name :

PD133.EXE	---> Write all EDID data and verify it.
PDO33.EXE	---> Write EDID data as following : serial number date code checksum
QA33.EXE	---> Read EDID data only.
DDC.WEK	---> Table of date code.
***.DDC	---> EDID data file.

(b) DDC.WEK format :

```
1995                    ----> year
03 07 11 15 20 24       ----> Table of week number from January to June.
29 33 37 42 46 50       ----> Table of week number from July to December.
1996                    ----> Next year
XX XX XX XX XX XX
XX XX XX XX XX XX       ----> Next year table
1997
XX XX XX XX XX XX
XX XX XX XX XX XX
:
:
:
:
```

(c) Data file format :

```
XX XX XX XX XX XX XX XX  --
:                        |
:                        | EDID data ( 128 bytes HEX code)
:                        |
                         --
XX          ----------->  Serial number ID
XXXXXXXX    ----------->  Manufacture name description
XXXXXXXX    ----------->  Product name description
XXXXXXXX    ----------->  CRT description
```

(3) Writer operation procedure

(a) PDI33.EXE operation :

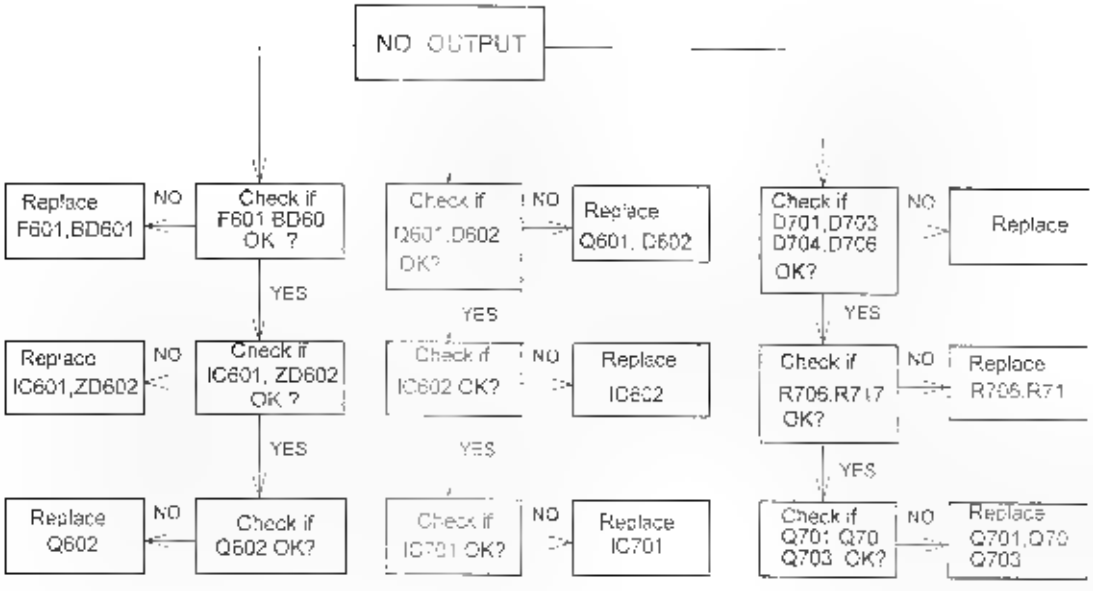
1. At DOS prompt enter "pdi33".
2. Flow command to enter data file name.
3. Input manufacture date. (OQI serial number only)
4. Ignore serial number, directly press 'enter' key.
   Otherwise, key in bar code number or use bar code reader to entry.
5. Turn off DDC monitor.
6. Turn on DDC monitor.
7. Press any key to continue.
8. Check result.

(b) PDO33.EXE operation :

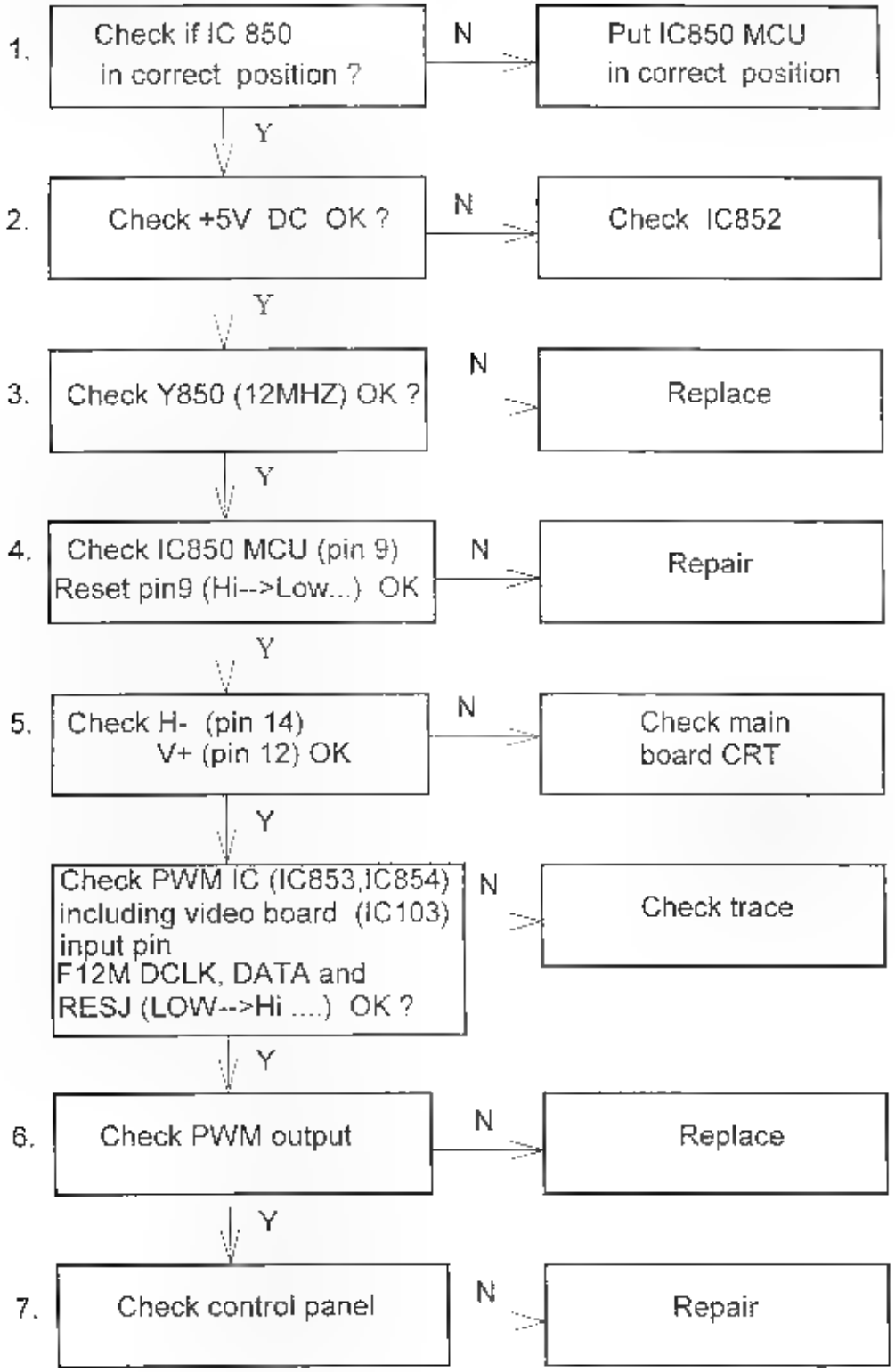
1. At DOS prompt enter "pdo33".
2. Flow command to enter data file name.
3. Input manufacture date. (OQI serial number only)
4. Key in bar code number or use bar code reader to entry.
5. Turn off DDC monitor.
6. Turn on DDC monitor.
7. Press any key to continue.
3. Input manufacture date. (OQI serial number only)
4. Key in bar code number or use bar code reader to entry.
5. Turn off DDC monitor.
6. Turn on DDC monitor.
7. Press any key to continue.
8. Check result.

TROUBLESHOOTING

4.1 No Output Power



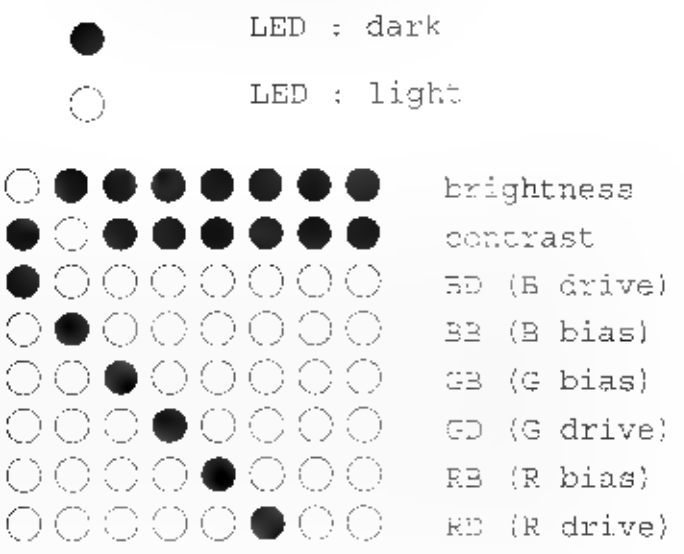
4.2 No Video MCU



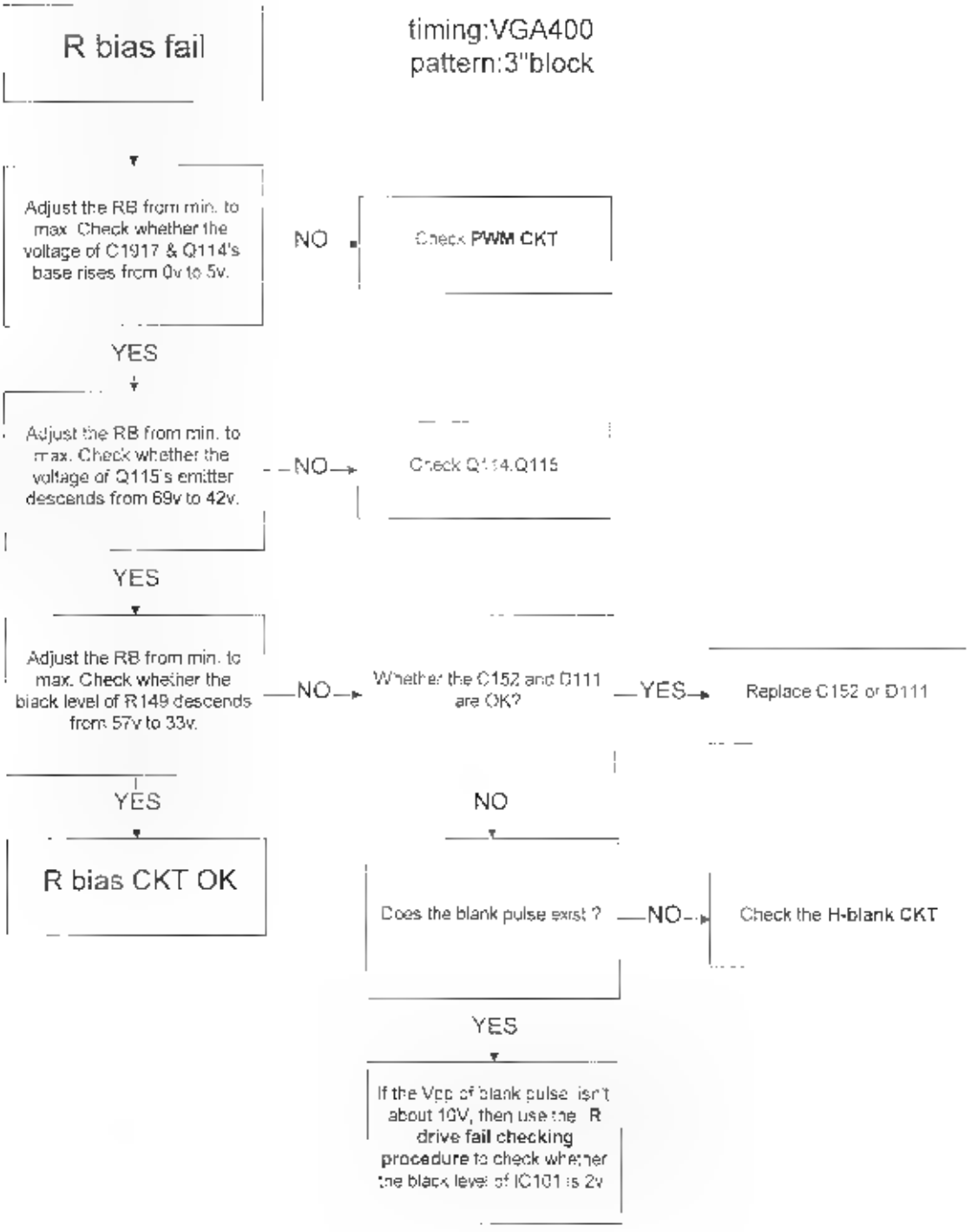
4.3 Video Troubleshooting

4.3.1 LED Define

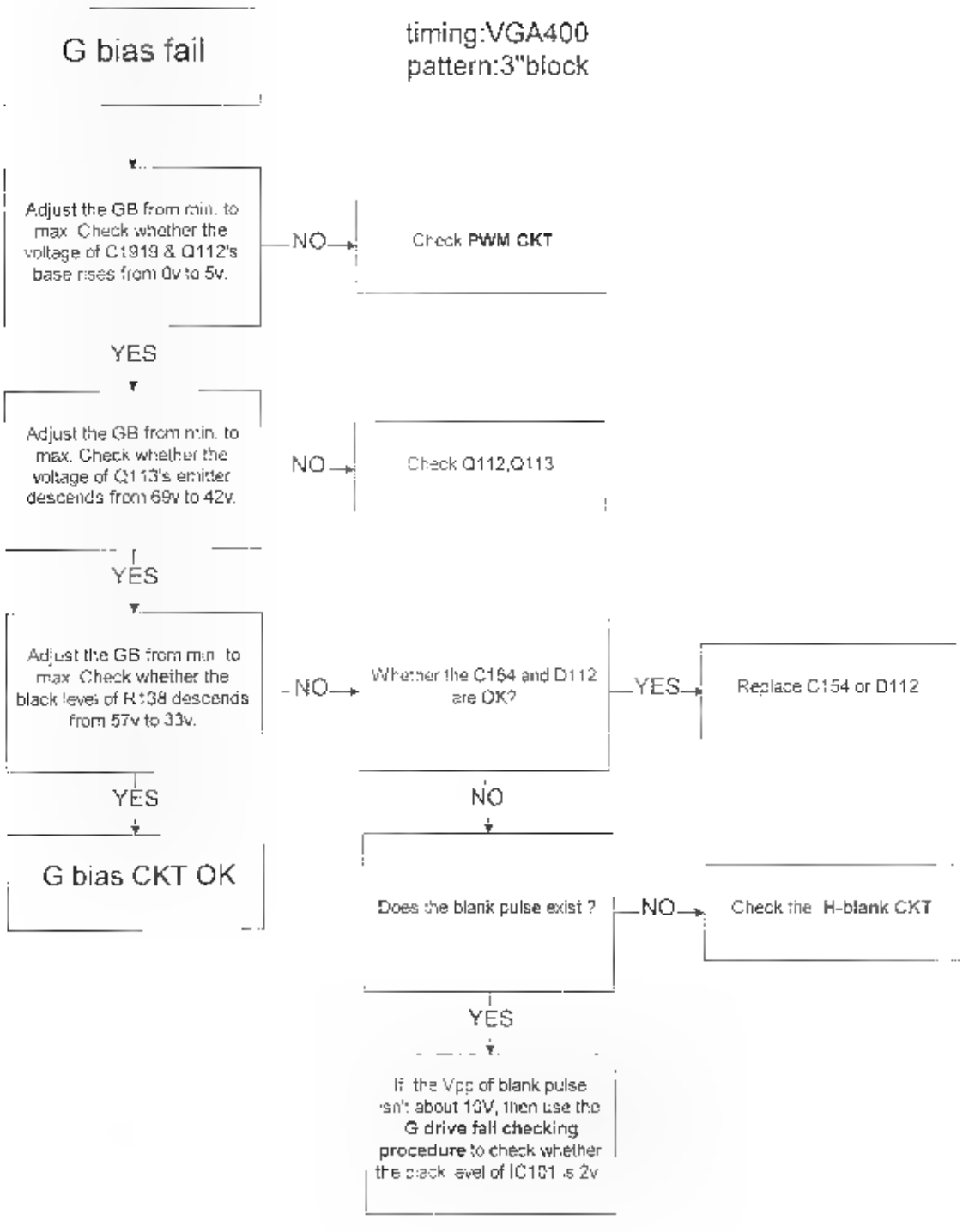
When the power is on, press the sel+ and adj- keys to enter the final checking mode. In the final checking mode the meaning of the LED's is defined as:



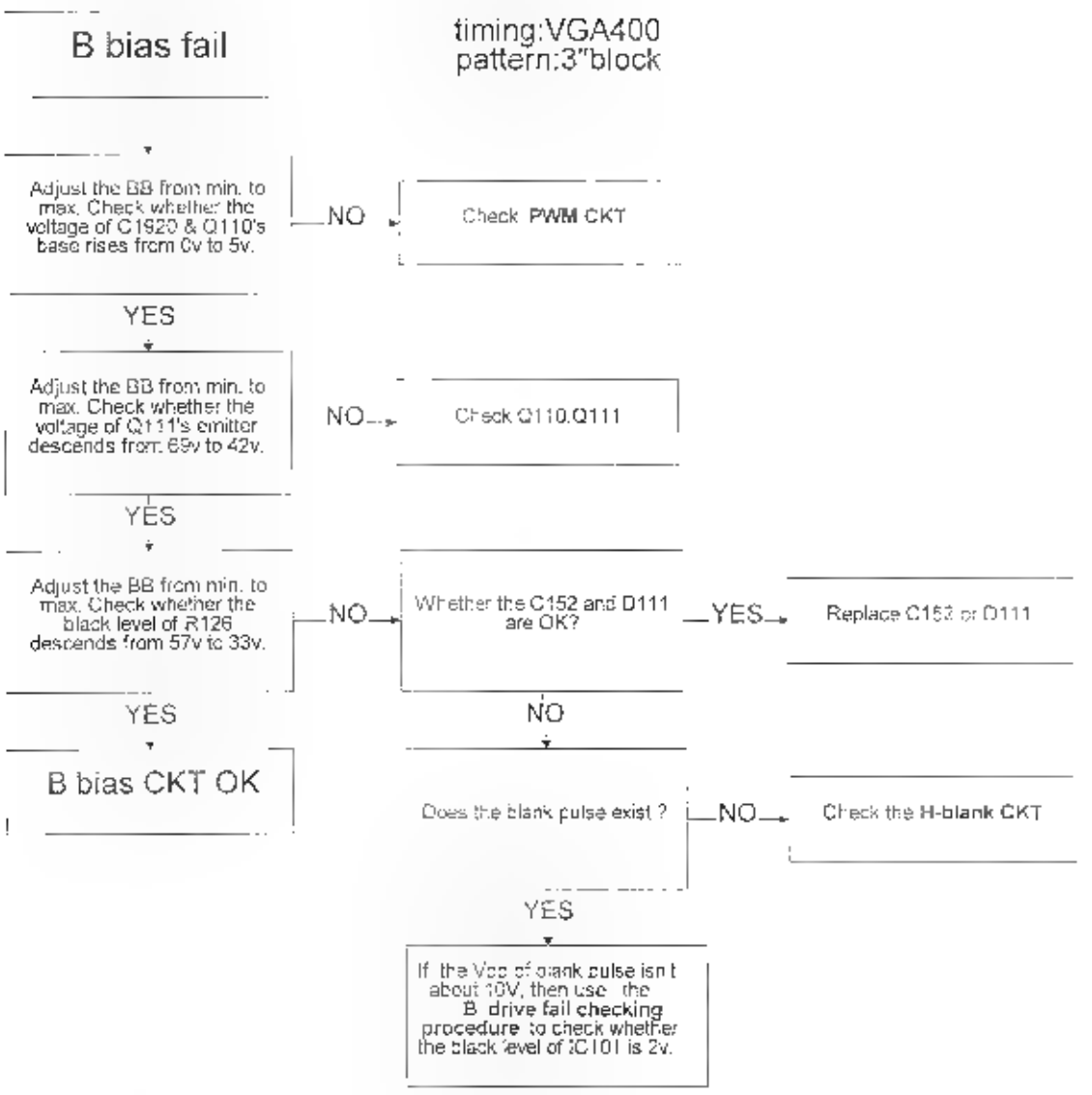
4.3.2 R Bias Fail



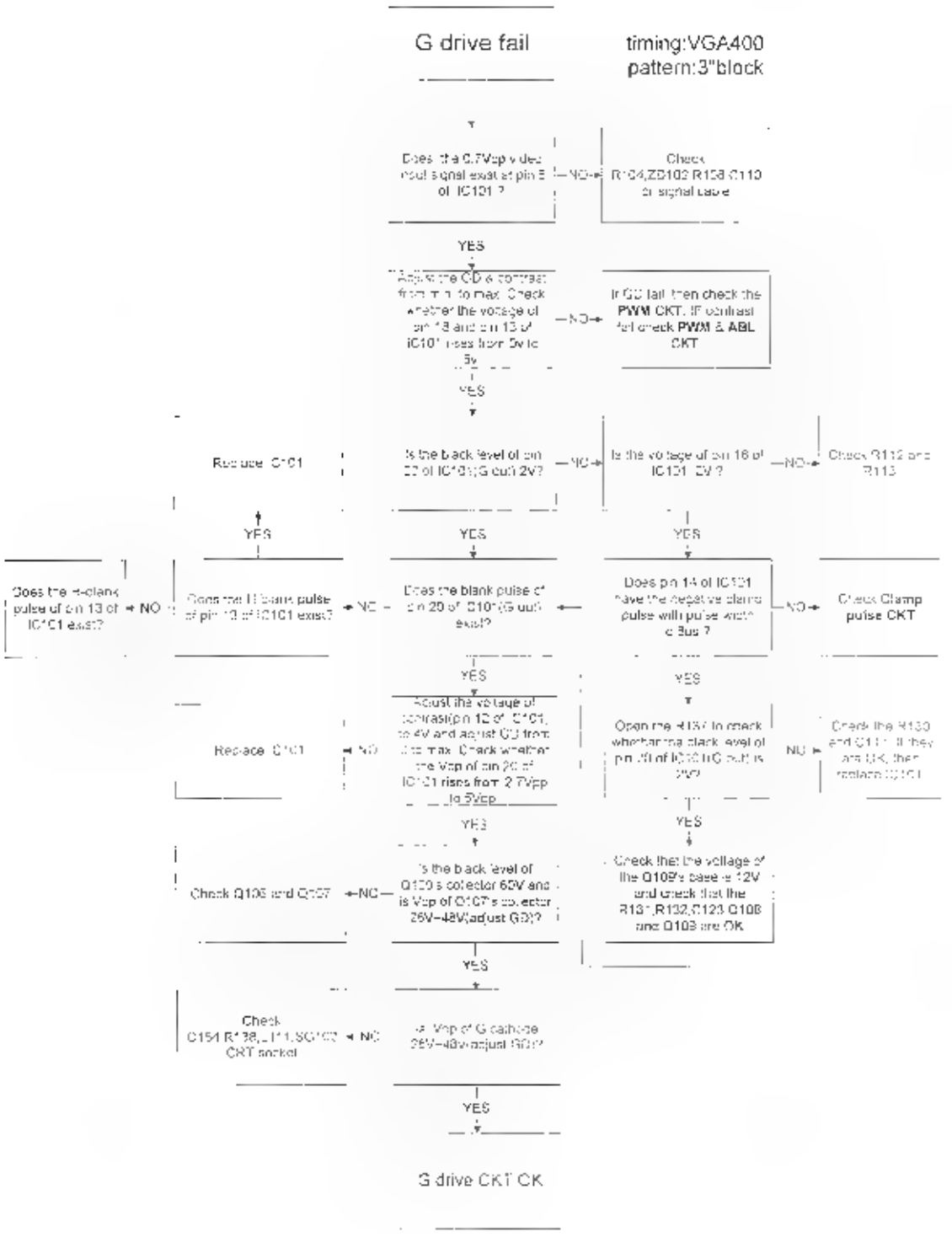
4.3.3 G Bias Fail



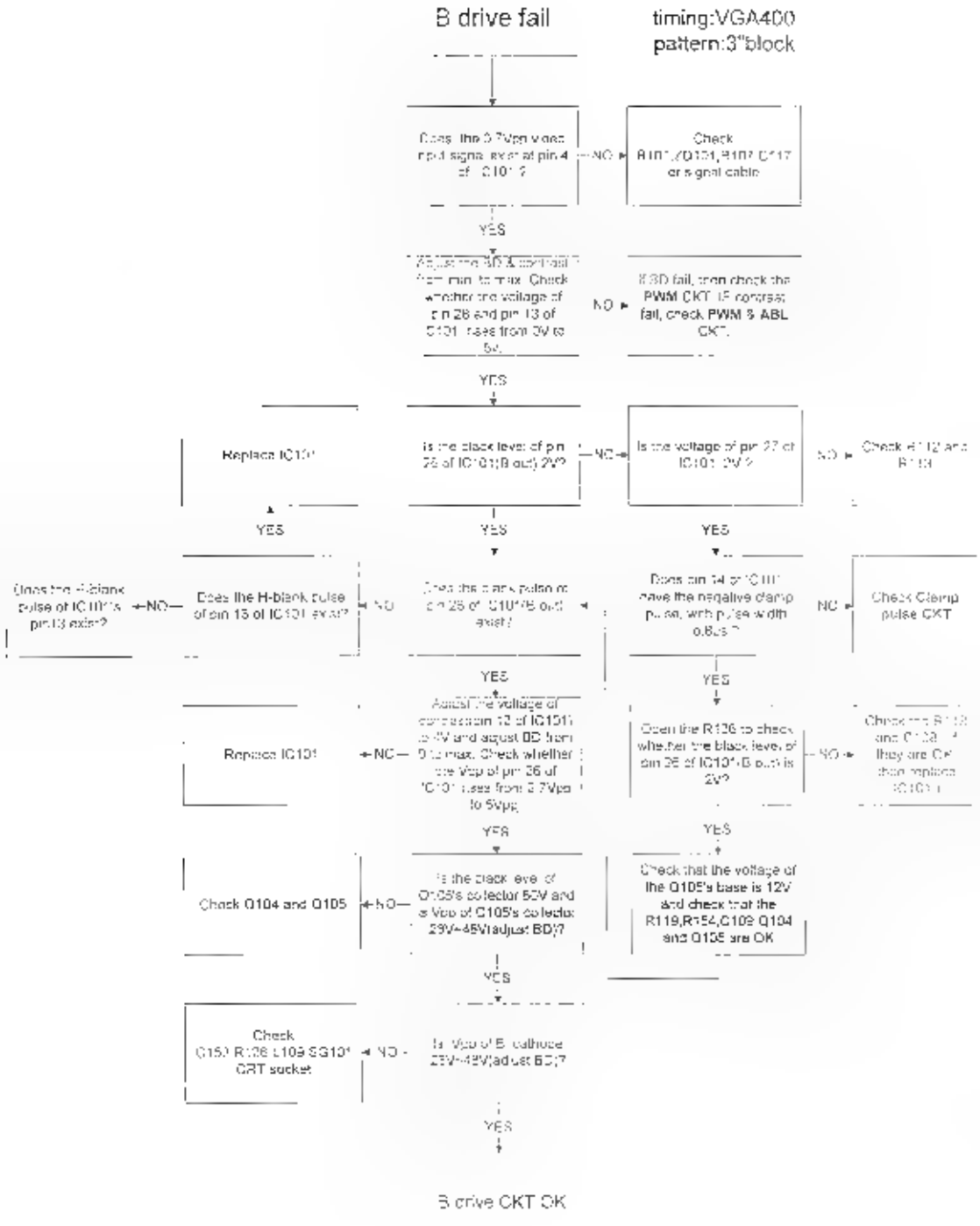
4.3.4 B Bias Fail



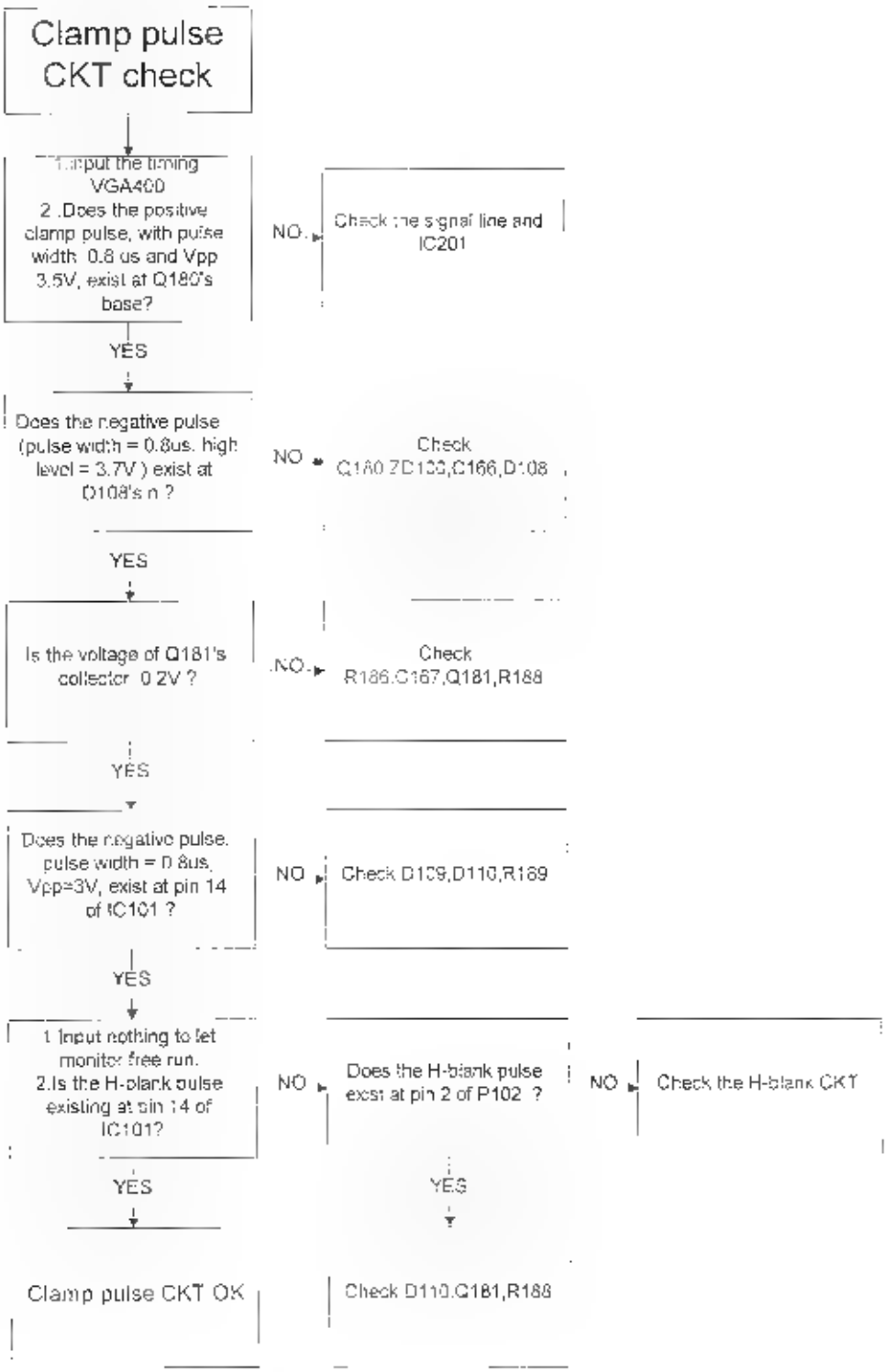
4.3.6 G Drive Fail



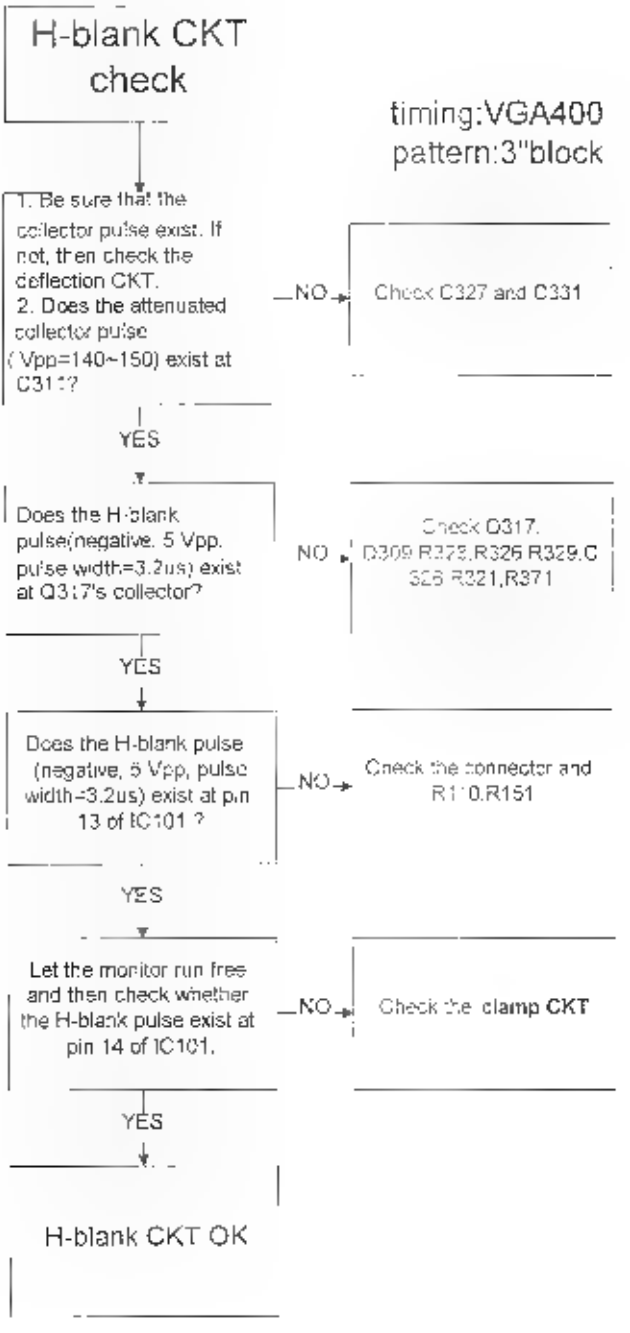
4.3.7 B Drive Fail



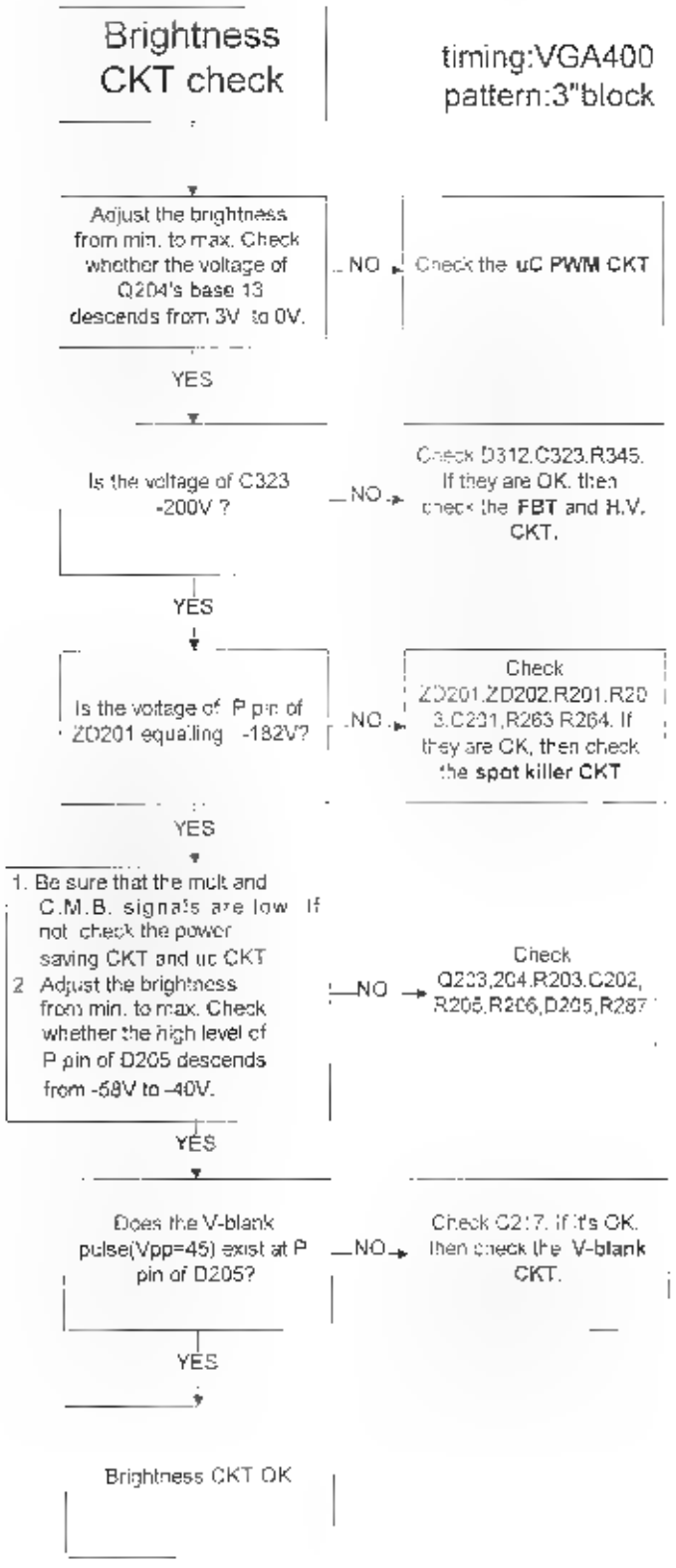
4.3.8 Clamp Pulse CKT Check



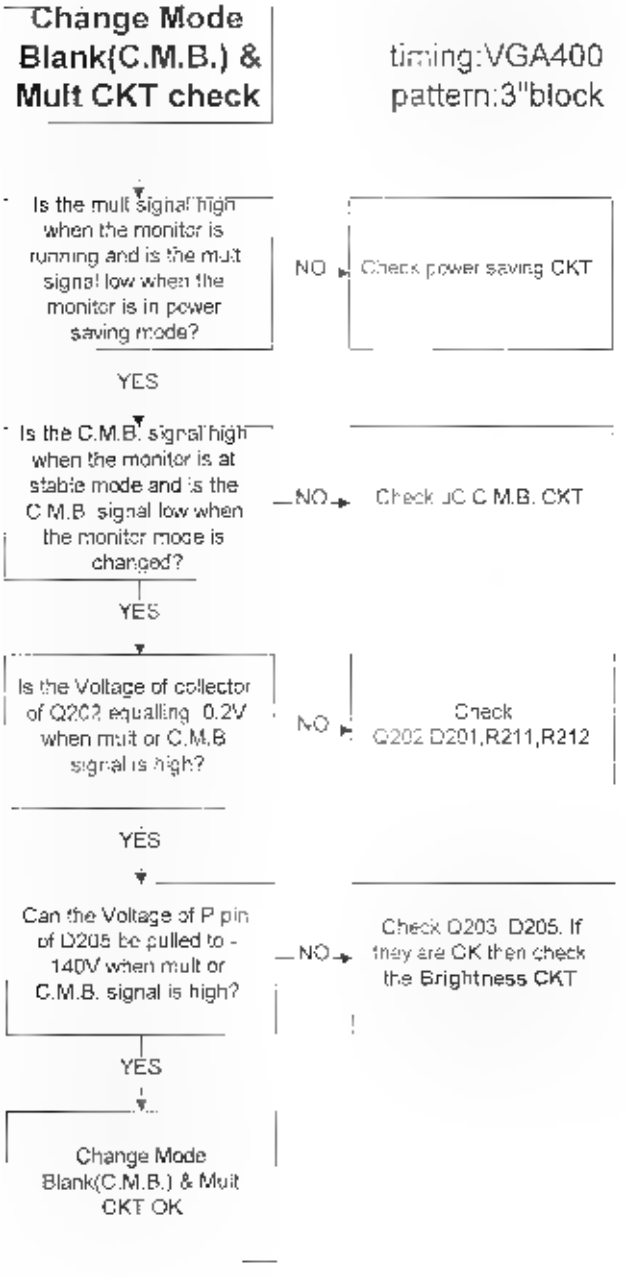
4.3.9 H-Blank Circuit Check



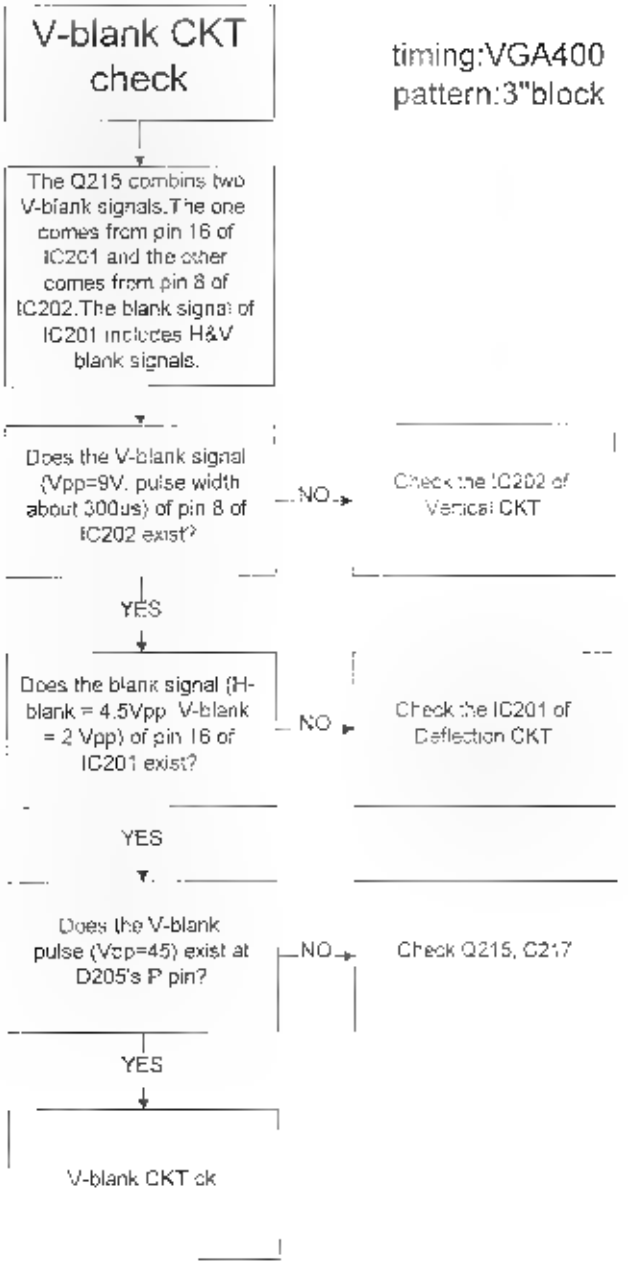
4.3.10 Brightness CKT Check



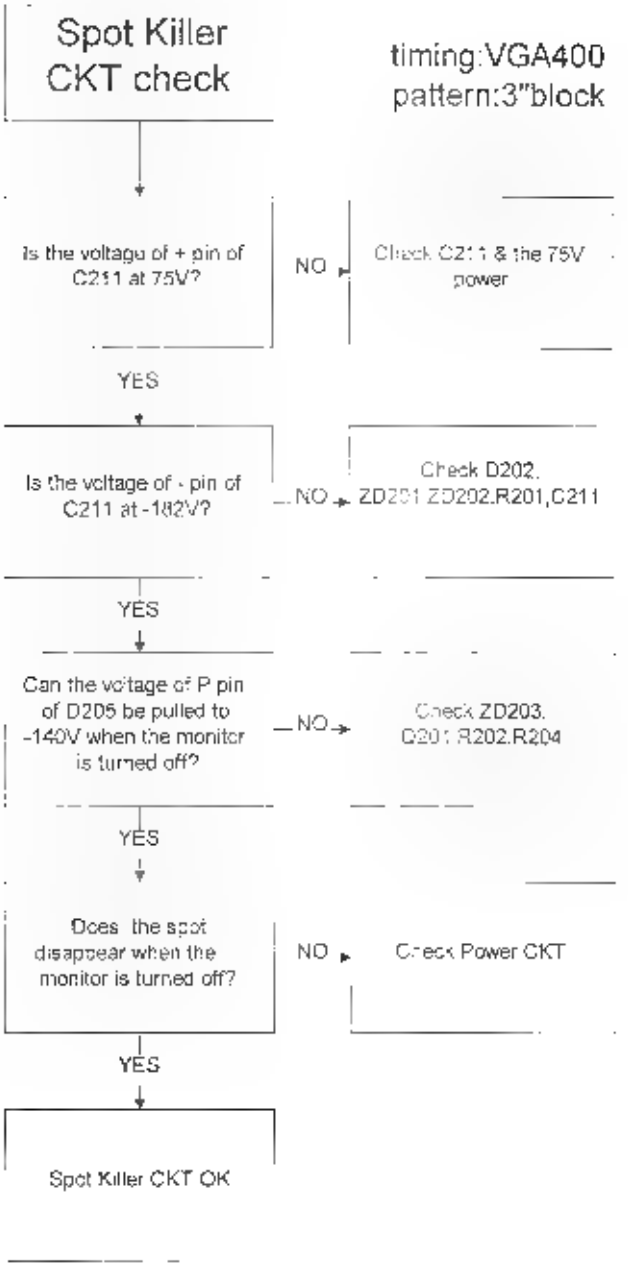
4.3.11 Change Mode Blank (C.M.B.) and Mult CKT Check



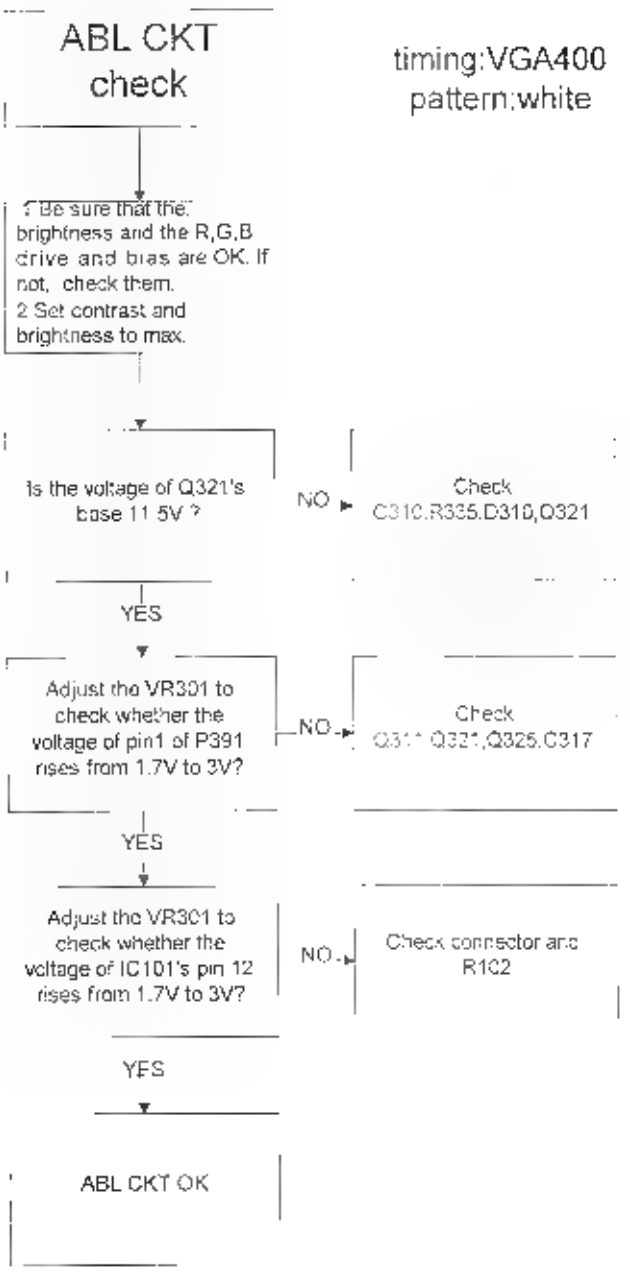
4.3.12 V-Blank Check



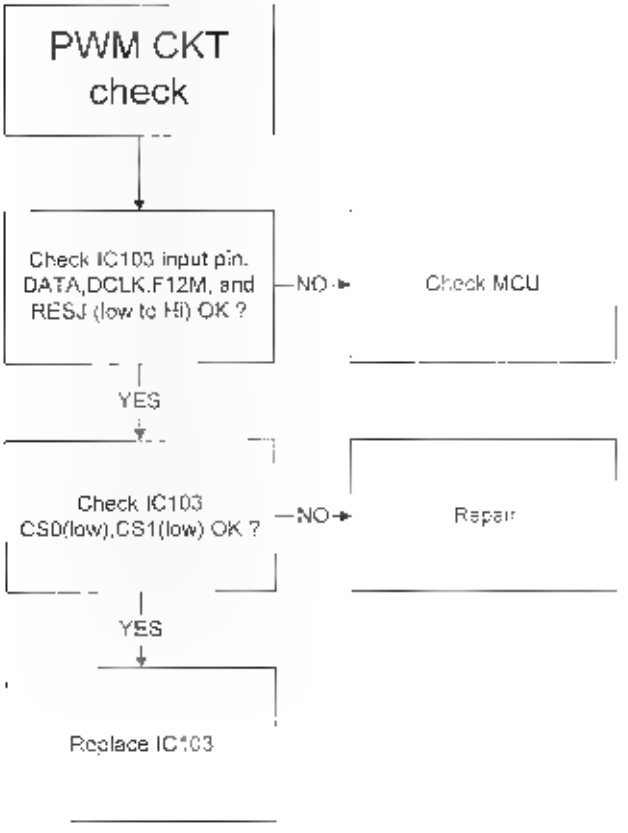
4.3.13 Spot Killer CKT Check

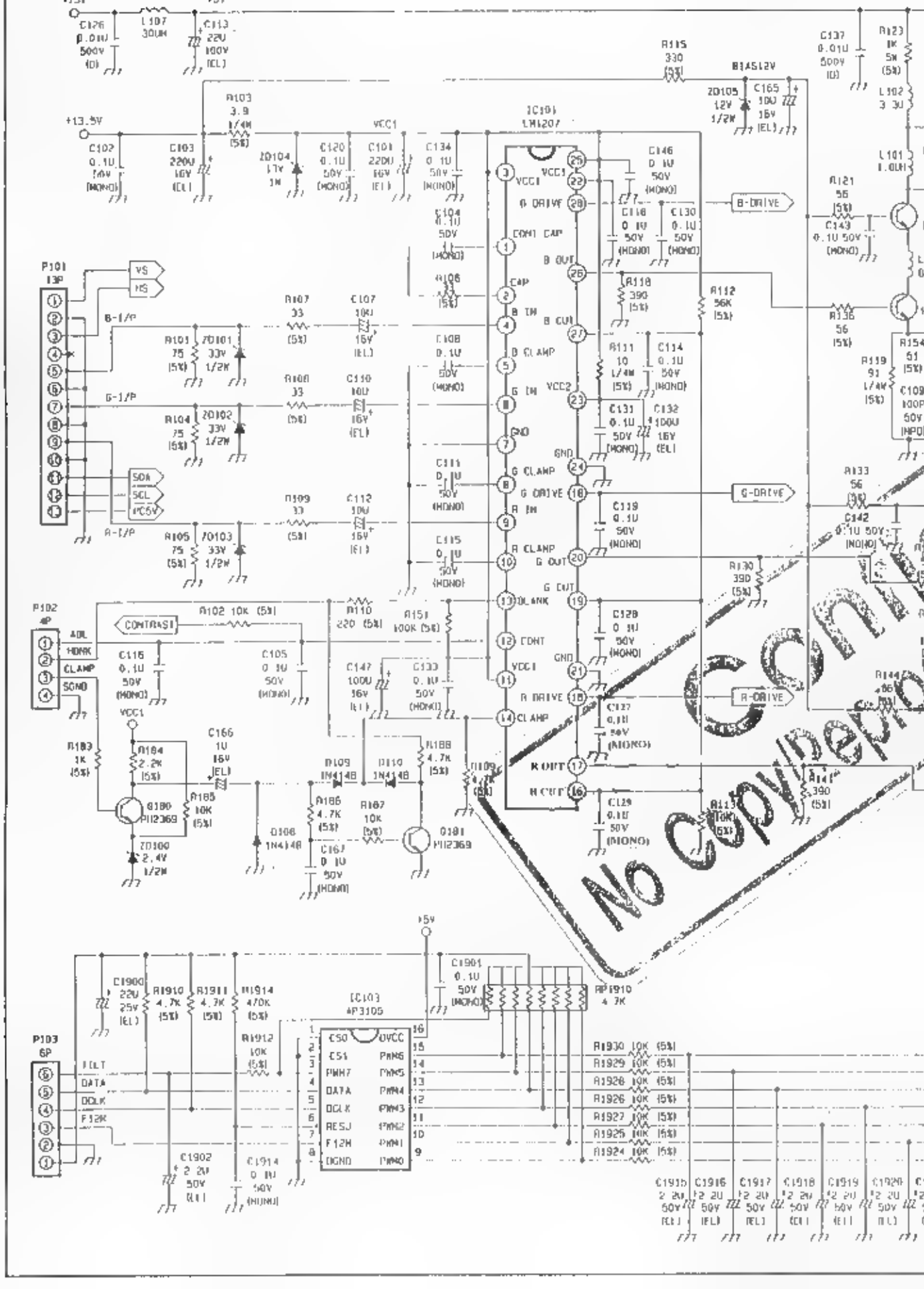


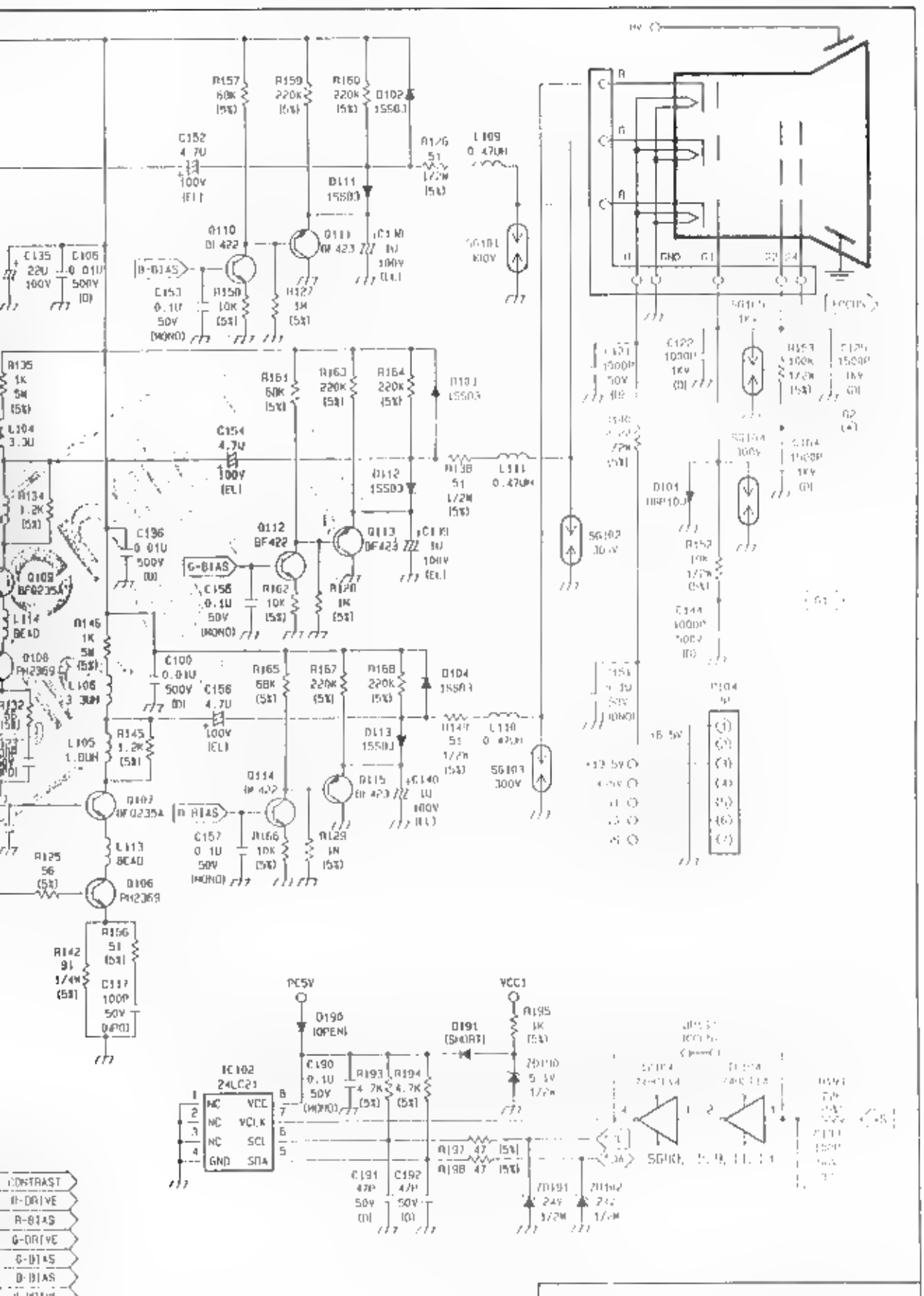
4.3.14 ABL Circuit Check



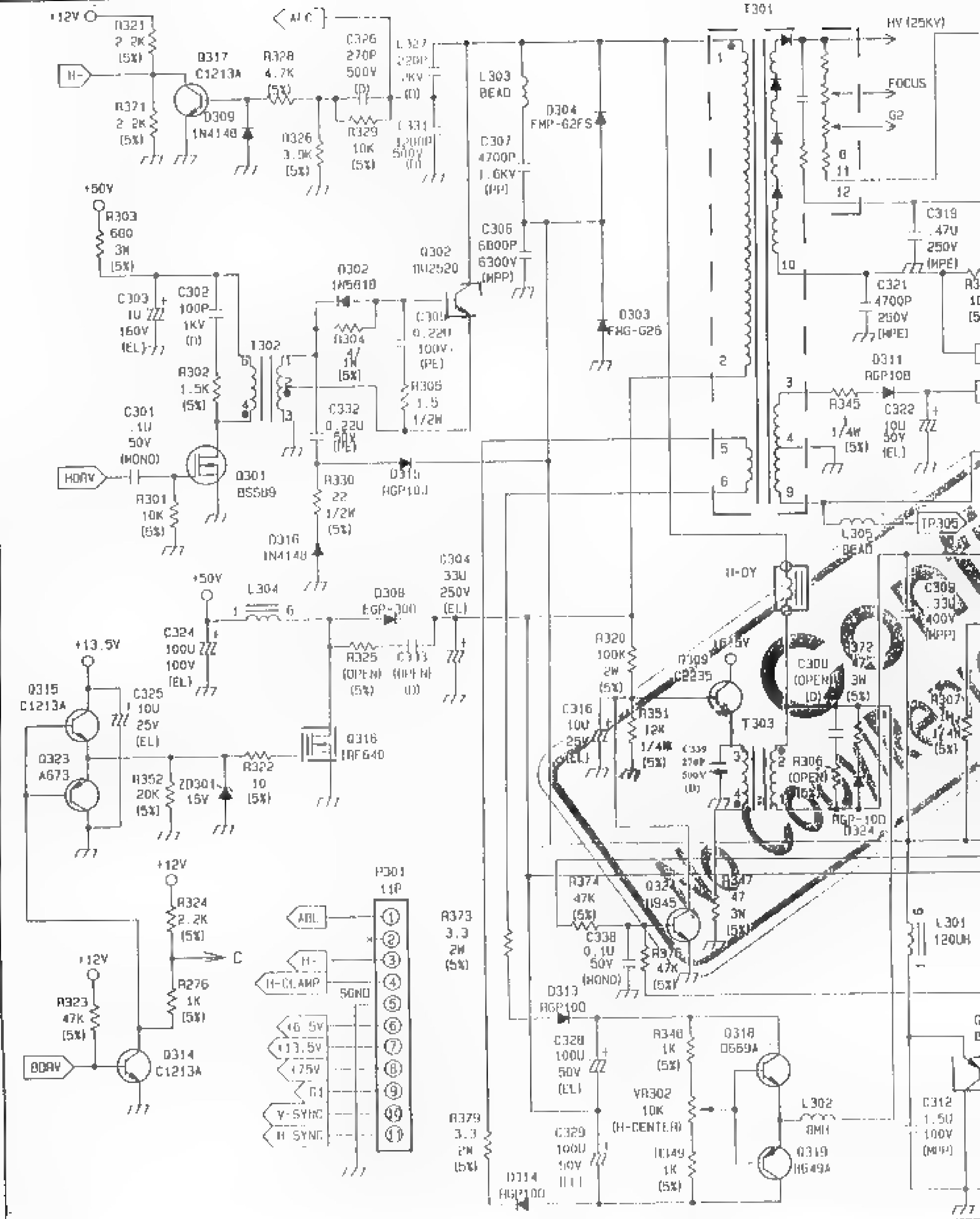
4.3.15 PWM CKT Check



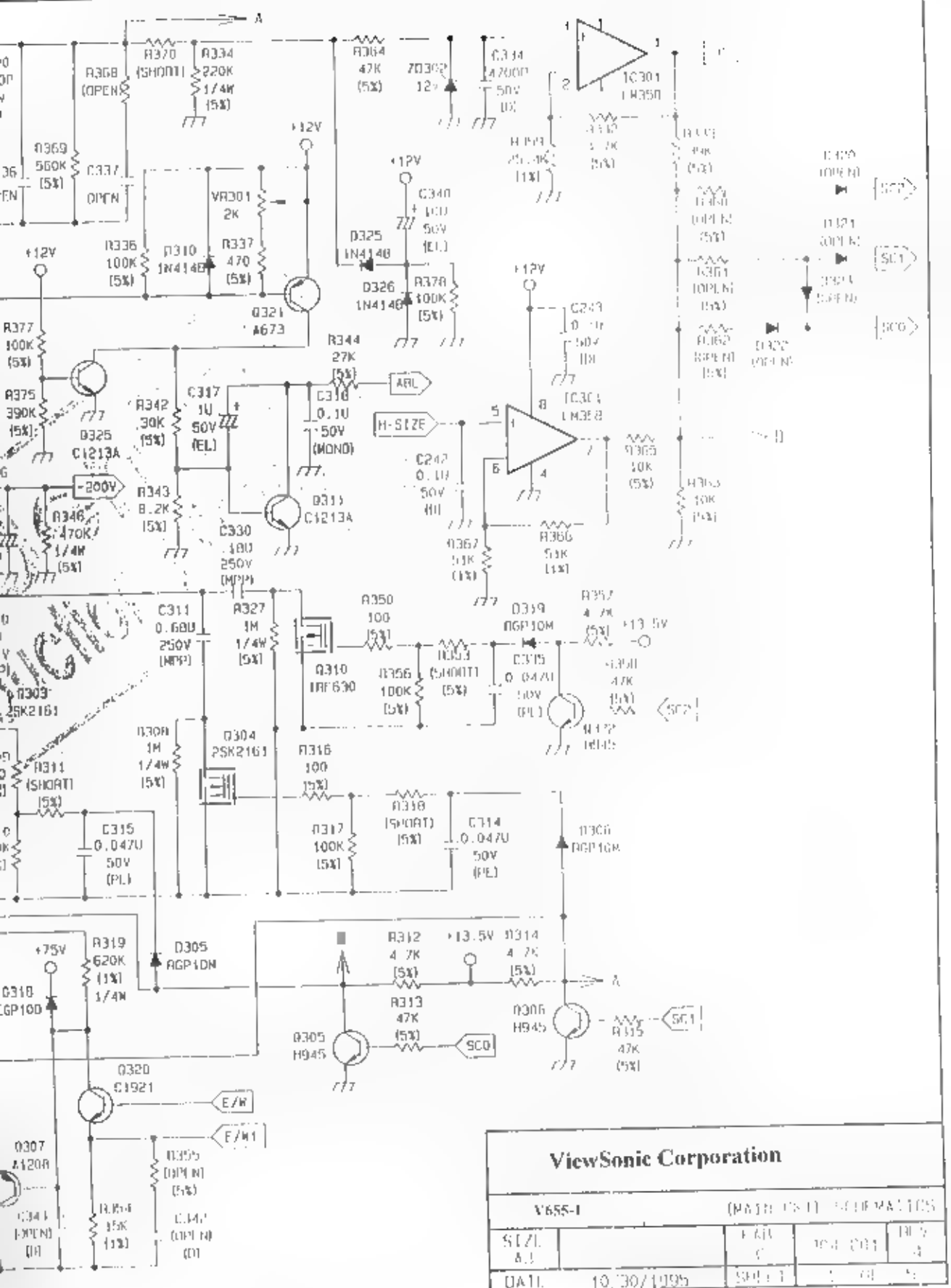

P101
13P
VS
HS
B-I/P
G-I/P
R-I/P
SDA
SCL
+5V
P102
4P
ADJ
HDRK
CLAMP
SGND
CONTRAST
P103
6P
FILT
DATA
DCLK
F12K
+13.5V
+5V
B1AS12V
IC101
LM1207
IC103
AP3105
VCC1
VCC2
GND
B DRIVE
G DRIVE
R DRIVE
B-DRIVE
G-DRIVE
R-DRIVE
B CLAMP
G CLAMP
R CLAMP
B IN
G IN
R IN
B OUT
G OUT
R OUT
BLANK
CONT
CAP
COM1 CAP
Q180
2SC2369
Q181
2SC2369
D108
1N4148
D109
1N4148
D110
1N4148
ZD100
2.4V
1/2W
ZD101
33V
1/2W
ZD102
33V
1/2W
ZD103
33V
1/2W
ZD104
17V
1W
ZD105
12V
1/2W
No Copyright



ViewSonic Corporation			
V655-1			
SIZE A1		PART 0	304
DATE: 10/30/1998		SHEET	



+12V
R321 2.2K (5%)
H-
R371 2.2K (5%)
Q317 C1213A
D309 1N4148
R328 4.7K (5%)
AFC
C326 270P 500V (D)
R326 3.9K (5%)
R329 10K (5%)
L327
C331 1200P 500V
L303 BEAD
C307 4700P 1.6KV (PP)
D304 FMP-G2FS
T301
HV (25KV)
FOCUS
G2
C306 6800P 6300V (MPP)
D303 FMG-G26
C319 .47U 250V (MPE)
C321 4700P 250V (MPE)
+50V
R303 680 3W (5%)
C303 1U 160V (EL)
C302 100P 1KV (D)
R302 1.5K (5%)
T302
D302 1N5818
R304 47 1W (5%)
Q302 11Q2520
C305 0.22U 100V (PE)
R305 1.5 1/2W
C332 0.22U 50V (PE)
C301 .1U 50V (MONO)
HDRV
Q301 BS589
R301 10K (5%)
R330 22 1/2W (5%)
D315 RGP10J
D316 1N4148
D311 RGP10B
R345 1/4W (5%)
C322 10U 50V (EL)
L305 BEAD
TP305
H-DY
+50V
L304
C324 100U 100V (EL)
D308 EGP-30D
C304 33U 250V (EL)
R325 (OPEN) (5%)
C313 (OPEN) (D)
R320 100K 2W (5%)
Q309 C2235
C309 .33U 400V (MPP)
C300 (OPEN) (D)
R372 3W (5%)
+13.5V
Q315 C1213A
C325 10U 25V (EL)
Q323 A673
Q316 IRF640
R352 20K (5%)
ZD301 15V
R322 10 (5%)
C316 10U 25V (EL)
R351 12K 1/4W (5%)
T303
R306 (OPEN)
RGP-10D
D324
+12V
R324 2.2K (5%)
C
R276 1K (5%)
+12V
R323 47K (5%)
BDRV
Q314 C1213A
P301 11P
ABL
H-
H-CLAMP
SGND
+6.5V
+13.5V
+75V
R1
V-SYNC
H-SYNC
R373 3.3 2W (5%)
R374 47K (5%)
C338 0.1U 50V (MONO)
R376 47K (5%)
R347 47 3W (5%)
L301 120UH
D313 RGP10D
C328 100U 50V (EL)
R348 1K (5%)
Q318 D669A
VR302 10K (H-CENTER)
L302 8MH
R349 1K (5%)
Q319 B649A
C329 100U 50V (EL)
D314 RGP10D
R379 3.3 2W (5%)
C312 1.5U 100V (MPP)



ViewSonic Corporation			
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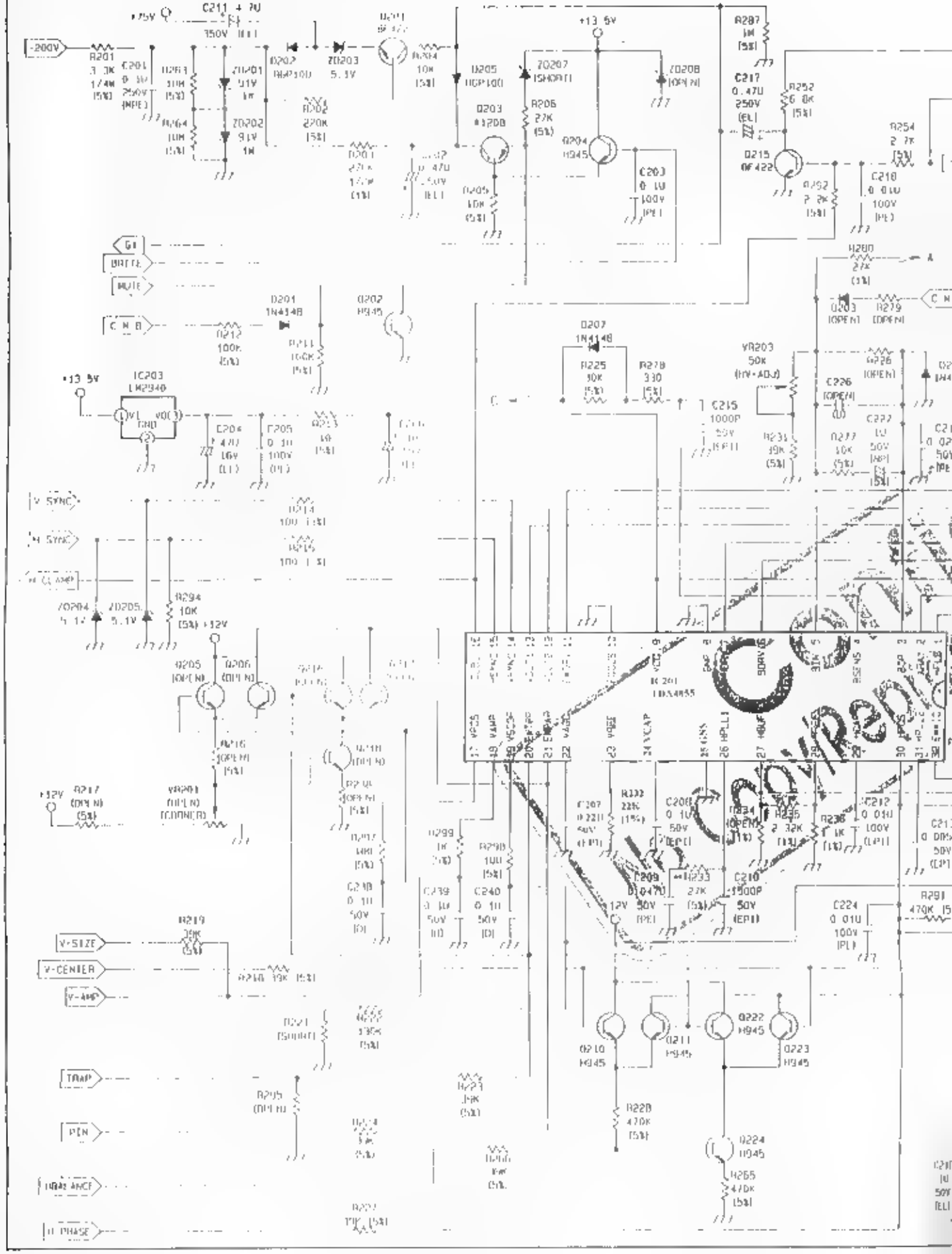
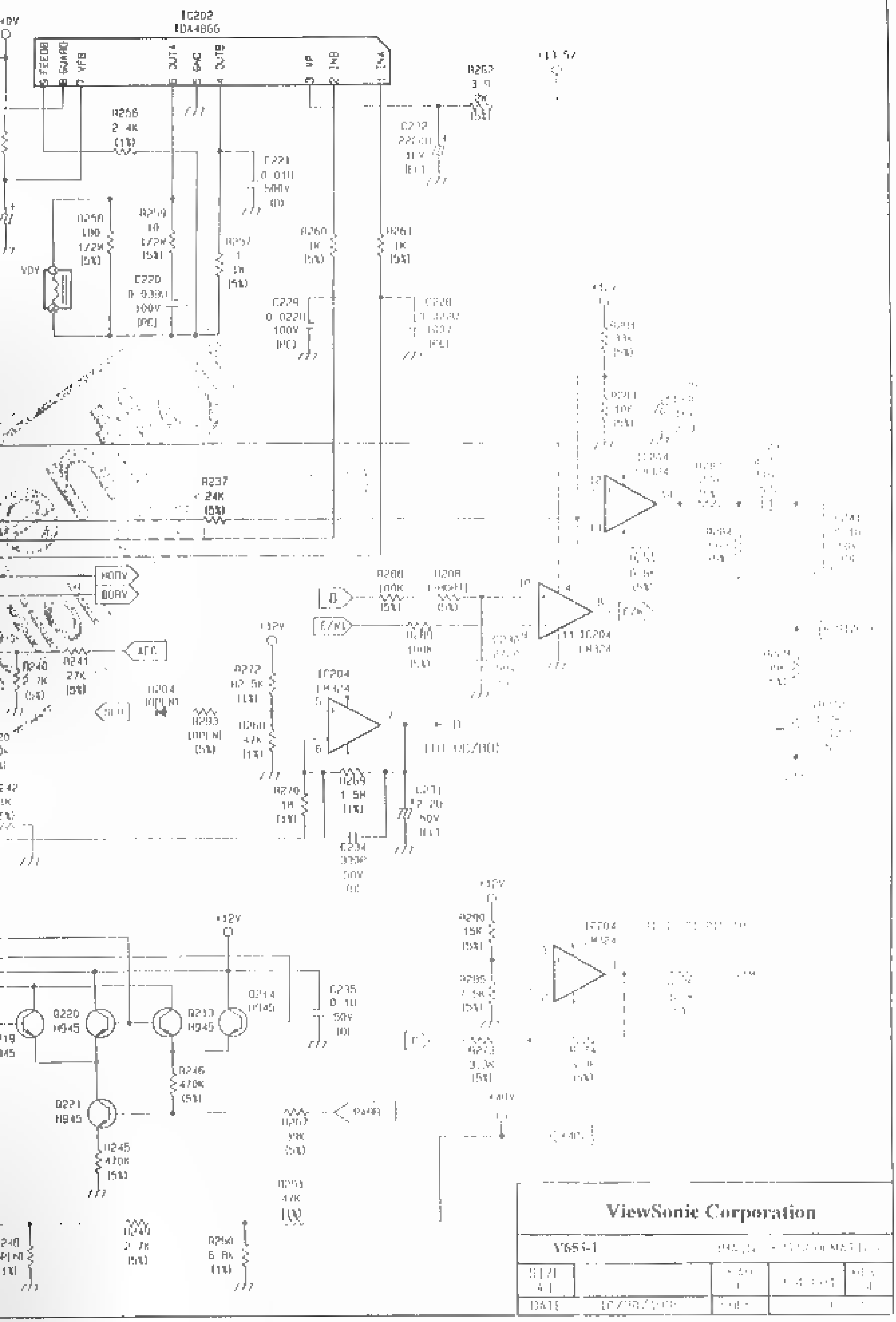
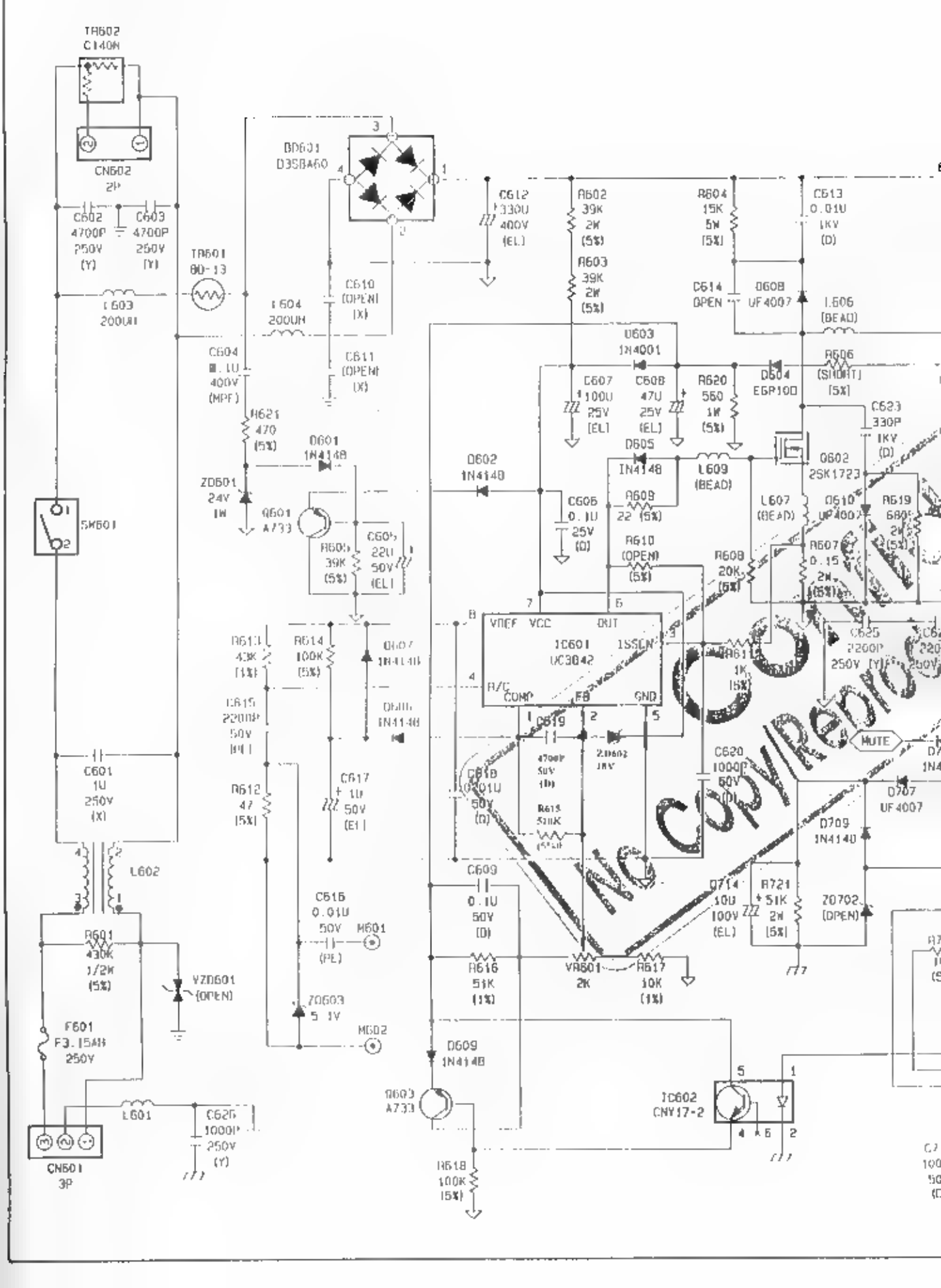
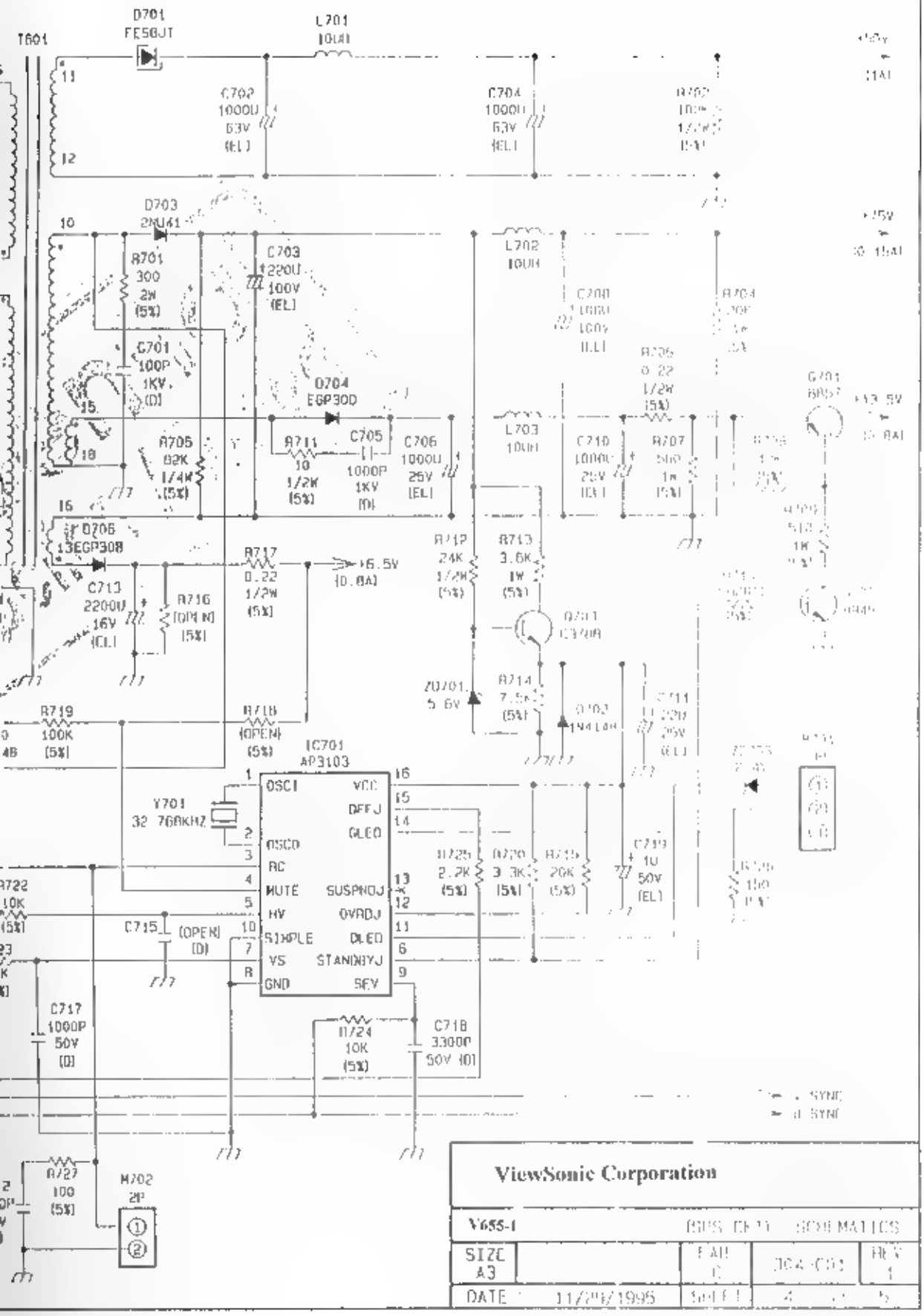



IC202
TDA4866
FEEDB
GUARD
VFB
OUT A
GAC
OUT B
VP
INB
INA
R262
R256
2.4K
(1%)
C221
0.01U
500V
R258
100
1/2W
(5%)
R259
1/2W
(5%)
VDY
C220
0.039U
100V
(PE)
R257
(5%)
R260
1K
(5%)
R261
1K
(5%)
C229
0.022U
100V
(PE)
R237
24K
(5%)
HDDV
BDRV
R268
100K
(5%)
R208
AFC
R241
27K
(5%)
R240
(5%)
R272
82.5K
(1%)
IC204
LM324
R204
R293
(5%)
+12V
R270
1K
(1%)
R269
1.5K
(1%)
C234
330P
50V
C271
50V
IC204
LM324
+12V
R290
15K
(5%)
R295
(5%)
+12V
Q220
H945
Q213
H945
Q214
H945
C235
0.1U
50V
R246
470K
(5%)
Q221
H945
R245
470K
(5%)
R249
(5%)
R250
6.8K
(1%)
ViewSonic Corporation
V655-1
DATE





ViewSonic Corporation

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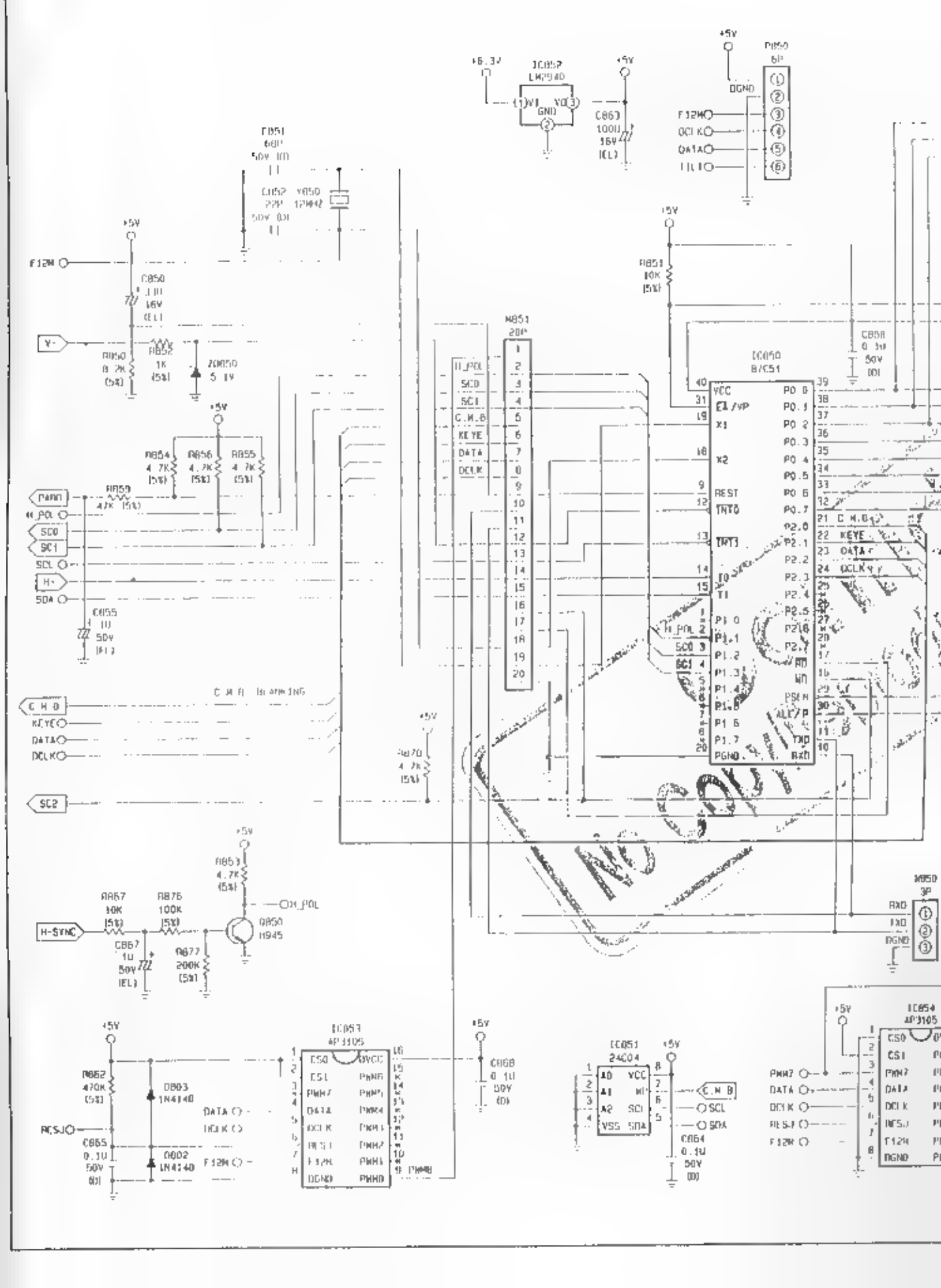
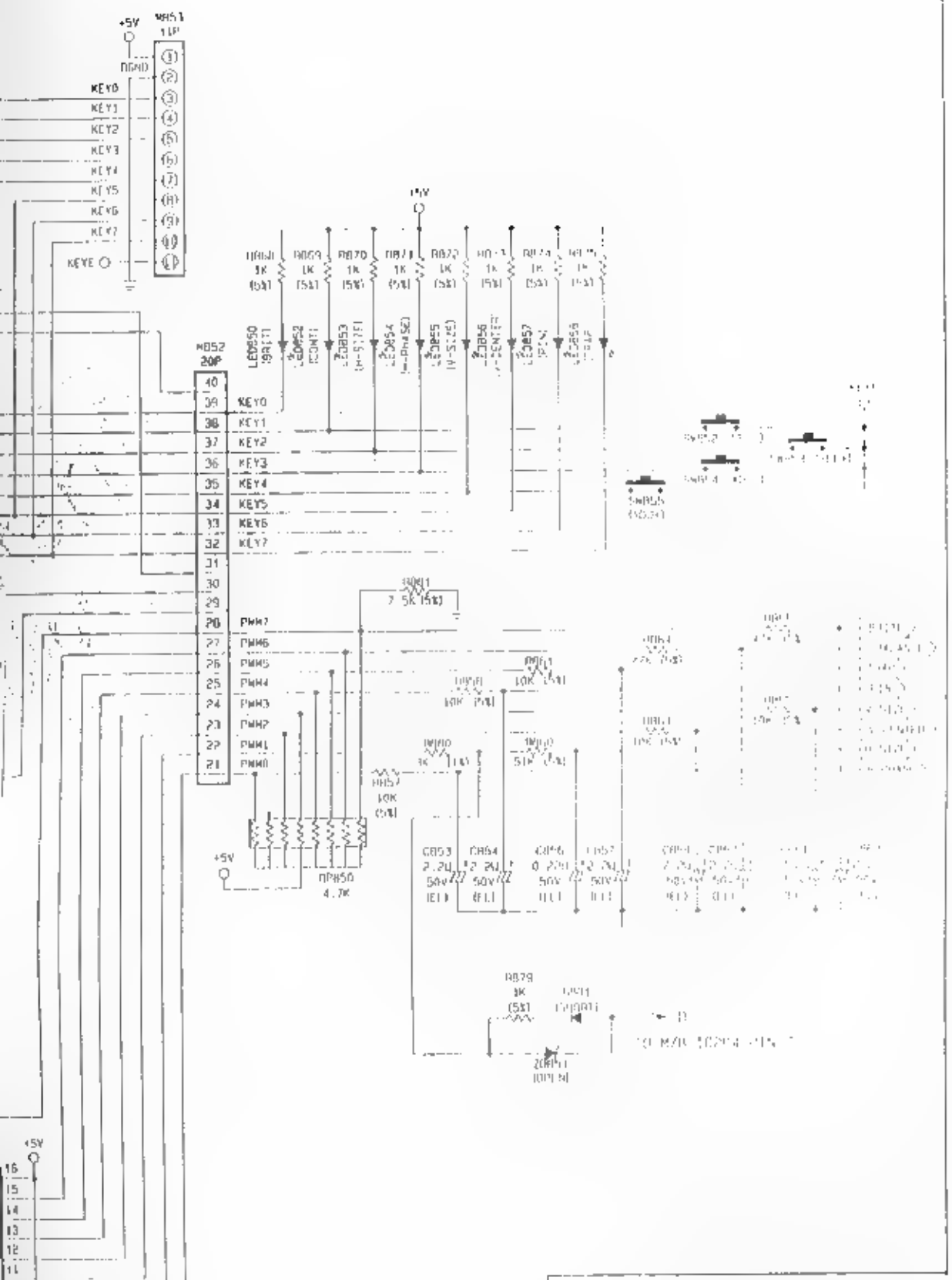
DATE 11/21/1995		SHEET 4		





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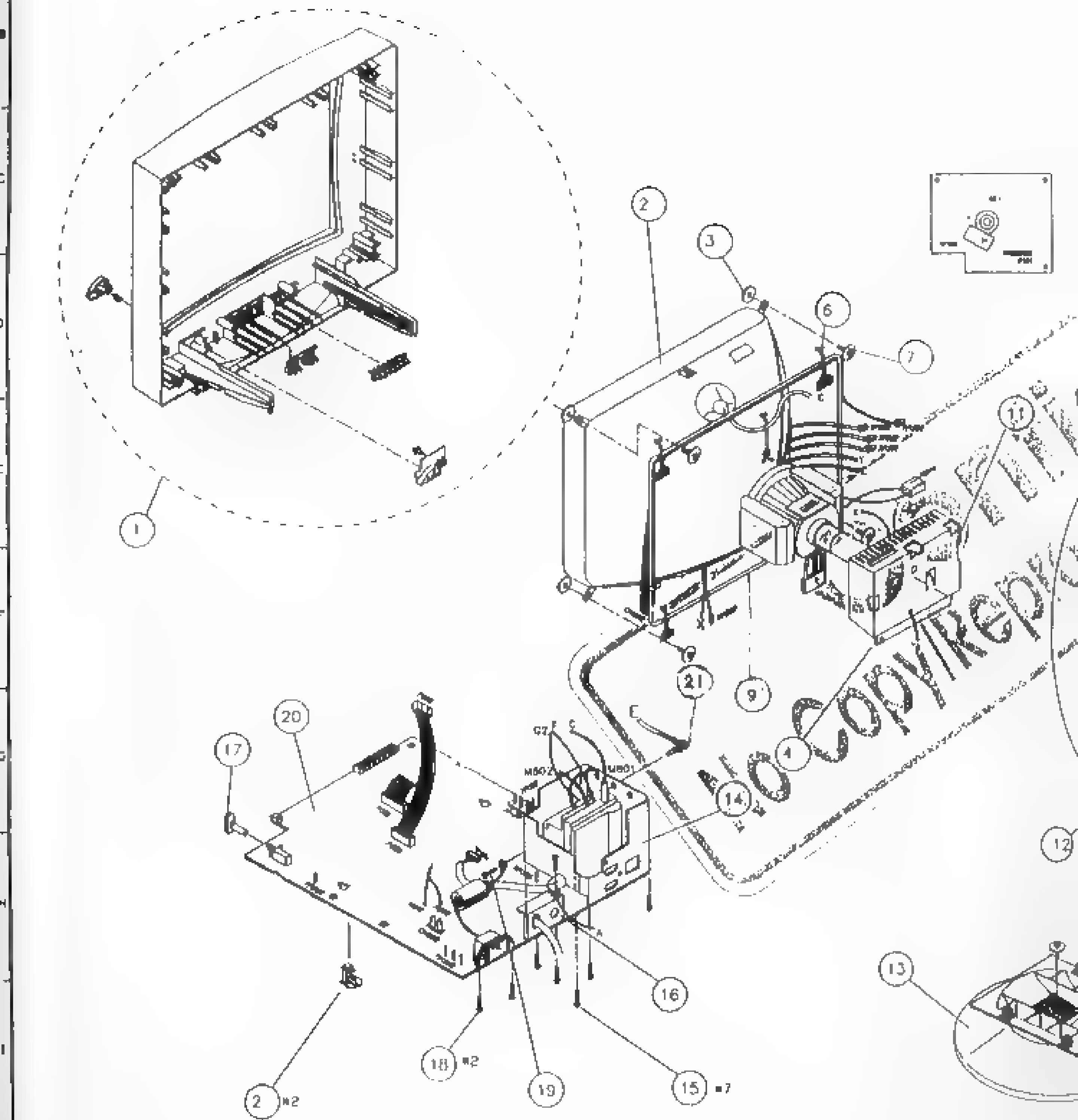
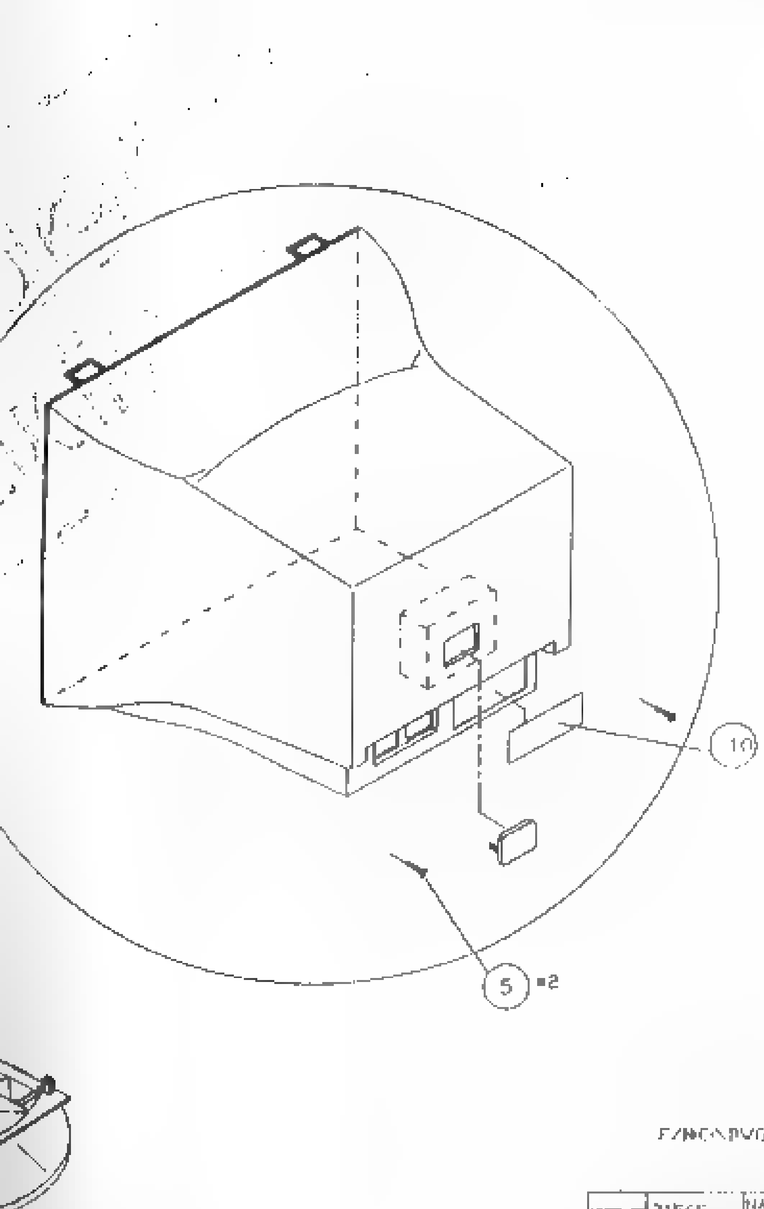

1
2
3
6
7
11
9
21
4
14
12
13
20
17
16
18 ×2
19
15 ×7
2 ×2
M802
M801
C2

ITEM NO.	PART NO.	DESCRIPTION	QTY
1	[illegible]	ASSY BEZEL	[illegible]
[illegible]	[illegible]	CRT 17"	[illegible]
[illegible]	[illegible]	SPACER CRT	[illegible]
[illegible]	[illegible]	PCB ... CRT	[illegible]
[illegible]	[illegible]	SCREW TAP ...	[illegible]
[illegible]	[illegible]	CLIP DEGAUSSING COIL	[illegible]
[illegible]	[illegible]	SCREW TAP WASHER ...	[illegible]
[illegible]	[illegible]	SPACER	[illegible]
[illegible]	[illegible]	DEGAUSSING COIL	[illegible]
[illegible]	[illegible]	LABEL ...	[illegible]
[illegible]	[illegible]	PHILLIPS ...	[illegible]
[illegible]	[illegible]	ASSY UPPER CASE	[illegible]
[illegible]	[illegible]	ASSY BASE	[illegible]
[illegible]	[illegible]	...	[illegible]
[illegible]	[illegible]	SCREW TAP ...	[illegible]
[illegible]	[illegible] [illegible]	ASSY REAR ...	[illegible]
17	[illegible]	...	[illegible]
[illegible]	[illegible]	SCREW TAP ...	[illegible]
[illegible]	[illegible]	SCREW ...	[illegible]
20	[illegible]	MAIN PCB	[illegible]



E:\NC\DWG\CA756E\DI.DWG

UNITS OF ASSEMBLY	7156E ACER	NAME ASSY DRAWING	
DRN	... LUO		
DSN	PETER WU		
CKD			
APPD		ViewSonic Corporation	
DRAWING NO.	57.76B02.002		

9 10 11 12 13 14 15

4.4 Spare Parts List

Part Number	Part Name	Location
27.81818.071	CORD SVT#18*3C 10A125V US 030	
42.77504.001	BAG PE HDPE 900*900 7076L/AMR	
44.76301.001	CTN AB 488*564*512 33S	
47.76301.001	CUSHION (L) EPS 7133S	
47.76302.001	CUSHION (R) EPS 7133S	
49.90028.001	COIL DEGAUSSING 7156IS W/O AL	
56.05761.061	CRT 15" M36KLH680X18(Q) LR	
59.76115.021	S.A. 1750MM 030 MULTI-MED W/COR	
60.77901.001	ASSY BASE 7133S	
60.76805.001	ASSY C CASE 030 7133S	
60.76804.001	ASSY BAZEL ABS 002	
55.76802.001	VIDEO BD 7156E	
01.03105.000	IC ASIC AP3105 PWMIC DIP 16P	IC103
02.02421.000	IC EEPROM 24LC21	IC102
03.07414.110	IC TTL 74HCT14	IC104
04.01207.010	IC VIDEO AMP LM1207	IC101
06.00422.010	XTOR BF422	Q110 112 114
06.00423.010	XTOR BF423	Q111 113 115
06.0235A.010	XTOR BFQ235A	Q105 109 107
06.02369.011	XTOR PH2369	Q181 180 104 108 106
13.10237.04E	RES CEM 1K J 5W	R123 135 146
18.R221W.12D	PEAK COIL 0.22UH M	L109
18.R471W.12D	PEAK COIL 0.47UH	L110 111
18.1R83W.12D	PEAK COIL 1.8U H	L101 103 105
18.4R73W.12D	PEAK COIL 4.7U H	L102 104 106
19.46020.001	CHOK 30UH 0.4D	L107
55.76802.001	MAIN BD 7156E	
01.03103.000	IC ASIC AP3103	IC701
01.03105.000	IC ASIC AP3105	IC853 854
01.08751.001	IC uCTRL CHMOS 87C51	IC850
02.02404.000	IC EEPROM 24C04	IC851
04.00324.010	IC OP LM324	IC204
04.00358.010	IC OP LM358	IC301
04.02940.03B	IC VR LM2940CT-12	IC203
04.03842.040	IC V.R. UC3842	IC601
04.04855.070	IC AUTO DEF CTRL TDA4855	IC201
04.05002.031	IC V.R. XC62AP5002LH	IC852
05.00017.010	IC OPTOCOUPLERS CNY17-2	IC602
06.00089.010	XTOR BSS89	Q301
06.00422.010	XTOR BF422	Q201 215
06.00630.020	FET MOS IRF630	Q310
06.00649.01A	XTOR 2SB649A	Q319
06.00669.01A	XTOR 2SD669A	Q318
06.00673.01A	XTOR 2SA673A	Q321 323
06.00733.011	XTOR 2SA733	Q601 603

06.00857.010	XTOR 2SB857	Q701
06.00945.010	XTOR H945	Q306 305 322 230 223 202 213 214 204 219 211 Q222 224 220 221 702 850 324
06.01208.011	XTOR 2SA1208	Q203 307
06.01213.01A	XTOR 2SC1213A	Q311 317 314 315 325
06.01921.010	XTOR 2SC1921	Q320
06.02235.010	XTOR 2SC2235	Q309
06.03788.010	XTOR 2SC3788	Q703
06.4R061.121	DIODE FMGG26 600V4A	D303
06.5R0F0.030	DIODE FMP-G2FS 1.5KV 5A	D304
17.10084.503	VR 50K	VR501
17.40010.202	SVR 2K	VR601
17.40016.103	SVR 10K	VR302
17.40016.104	SVR 100K	VR202
17.40016.202	SVR 2K	VR301
17.40016.503	SVR 50K	VR203
19.20079.001	XFORM EI-28 2MH 56E L304	L304
19.20079.011	XFORM EI-29 56L 1302	L302
19.20079.021	XFORM PWR EE 2015 T601 56F	T601
19.40067.001	LINE-FILTER 7.5MH	L602
19.40084.001	CHOKE 200UH	L604 603
19.40093.001	CHOKE 8MH	L302
19.46003.001	CHOK 10UH	L702 703 703
19.50034.001	COIL LINEAR T-03	T303
19.60041.001	XFORM EI-25 13-0 BT L302	L301
19.70035.011	TRANSFORMER FBT 7156E	T301
26.13151.113	FUSE 3.15A 250V S120	F601
04.04866.070	IC VERT DEF DRV TDA4866	IC202
06.00861.010	XTOR 2SB861	Q308
06.02161.020	FET MOS 2SK2161	Q303 304
06.00640.02A	FET MOS IRFS640	Q316
06.02520.010	XTOR BU2520AF S0T199 NPN	Q302
06.01723.020	FET MOS 2SK1723	Q602
55.76902.001	CTRL BD 7156S	
06.00036.142	LED D3*3.5 GRN DIFFUS FLANGE	LED801 802 803 804 805 806 807 808
06.03N5X.147	LED D3*5.3 GRN YEL KTL-3N5X	LED701

pyright

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rson of such revision or changes.

TABLE OF CONTENTS

System Overview

1.1 Introduction

This specification describes a low-cost high performance 15" color auto-scan monitor which operates with high-end Windows® and CAD/CAM applications. This intelligent monitor is microprocessor controlled, with a powerful memory base of pre-programmed screen and input configurations. The V655 also allows users to place their own settings into memory via external controls. It is compatible with various kind of computers and graphics adapters; it synchronizes automatically with the horizontal frequencies from 30kHz to 64 kHz (24.8 kHz is optional) and vertical scanning frequencies from 50Hz to 100Hz. When it operates on a 1024 x 768 resolution, the V655 maintains a 76Hz non-interlaced refresh rate for flicker-free high quality image to reduce eye strain.

The V655 has the following features:

-Energy saving function
-Suspend mode indicator with amber
-Off mode indicator with amber blinking
-Universal switching power supply
-0.28mm dot pitch CRT
-User controls: Power on/off, adjustment (+, -), Select, are all in front bezel
-Power on/off indicator
-Power on auto degaussing
-User setting indicator
-20 seconds auto save function
-12 factory preset modes memory partitions
-20 modes reserved for user setting
-Tilt and swivel base
-Detachable power cable
-VGA resolution at 31.5kHz

640 X 400
640 X 480

-8514/A resolution: 1024 X 768(interlaced) at 35.5kHz
-SVGA resolution: 800 X 600 from 34kHz to 48kHz
-UVGA resolution: 1024 X 768(non-interlaced) from 48kHz to 64kHz
-Automatic scanning all horizontal frequencies from 30kHz to 64kHz, and all vertical frequencies between 50Hz and 100Hz
-MPRII function

1.2 Operational Specification

1.2.1 Environment

Temperature

-Operating 10 to +40 degrees Celsius
-Non-operating -20 to +60 degrees Celsius
NOTE: If tested without packing, the maximum non-operating temperature is 52 degrees Celsius.

Humidity

-Operating 20% to 90% non-condensing
-Non-operating 10% to 95% non-condensing

Altitude

-Operating 0 to 3,048m (10,000 ft)
-Non-operating 0 to 12,192m (40,000 ft)
-Operating condition / without packing
-Non-operating condition / with packing

1.2.2 Electrostatic Discharge Requirements

The V655 must withstand 15KV test voltage of Electrostatic Discharge and meet the acceptance criteria.

1.2.3 Safety Requirements

The display unit complies with the following safety standards and specifications.

110V Version

-UL compliance....standard for information-processing and business equipment, UL 1950.
-CSA compliance...standard C22.2 No. 950-M89, data processing equipment.
-DHHS...rules 21 sub-chapter J as of date of manufacture.

220V Version

-TUV compliance...EN60950 safety specification-business equipment
-PTB...German X-ray emission standards.
-ZH1/618...German ergonomic standard.
-ISO9241-3...Ergonomic Requirements of Visual Display.
-Demko...EN60950.
-Nemko...EN60950.
-Semko...EN60950.
-Fimko...EN60950.

1.2.4 EMI Requirements

This display unit complies with the following RFI rules and regulations.

110V Version

-FCC compliance...FCC Rule, Part 15, Subpart B, Class B.
-VCCI compliance...VCCI Rule, Class-2.

220V Version

-BZT compliance...BZT regulations vfg. 243/1991 for RFI suppression, Class B.
-DNSF compliance...EN55022, Class B.
-Low Radiation...MPRII.

1.2.5 Acoustical Noise

When the display is in operation, the sound measurement shall be within 40 dB in the audible field.

1.2.6 Reliability

The MTBF of the display unit shall be greater than 40,000 hours excluding the picture tube.

1.3 Input / Output Signal Requirements

1.3.1 Input Signal Requirements

1.3.1.1 Signal Cable (directly attached to unit)

Video Inputs:

15-pin mini D-sub connector is on the captive signal cable for IBM VGA, 8514A or compatible graphics adapters. The pin assignments of this connector are as the following:

**15 pin mini D-sub male

1	RED VIDEO
2	GREEN VIDEO
3	BLUE VIDEO
4	GROUND
5	GROUND
6	RED GROUND
7	GREEN GROUND
8	BLUE GROUND
9	NO-CONNECTION
10	SYNC GROUND
11	GROUND
12	SDA
13	H.SYNC
14	V.SYNC
15	SCL

Cable Length:

Cable length 2000mm and audio cable at PC side 250mm.

1.3.1.2 Video Signal: Analog 0.7 Vpp/75 ohm positive.

1.3.1.3 SYNC Signal:

- Separate SYNC : TTL level.
- Horizontal SYNC : positive/negative.
- Vertical SYNC : positive/negative.